Parallel-Connected SiC MOSFETs – Essence, Challenges, and Solutions

Helong Li and Shuang Zhao

Hefei University of Technology

helong.li@hfut.edu.cn, shuang.zhao@hfut.edu.cn

Speakers' Biographies

Helong Li is currently a Professor at Hefei University of Technology. He received B.Sc. and M.Sc. degree in Electrical Engineering from Harbin Institute of Technology, in 2010 and 2012, respectively, and received the Ph.D. degree from Aalborg University, Denmark, in 2015. From 2016 to 2019, he worked at Dynex Semiconductor Ltd, as Senior and Principal R&D Engineer, for power semiconductor packaging, testing, reliability. From 2019 to 2021, he worked at CREE Europe GmbH in the field of SiC automotive applications. He supported mainstream automotive customers in Europe and has good insight on SiC power modules in automotive applications. Since 2021, he has been with Hefei University of Technology as a professor in power electronics, mainly focusing on power semiconductor packaging and applications. Dr. Li has received Hubing Scholar from Hefei University of Technology in 2022. He published more than 50 scientific papers. Dr. Li also participated in the definition of automotive standard AQG324 for SiC power modules.

Shuang Zhao is currently an Associate Professor at Hefei University of Technology. He receives BSEE and MSEE from Wuhan University, Wuhan, China in 2012 and 2015 respectively, and obtains his PhD degree from University of Arkansas, Fayetteville, AR, USA in 2019. He was an intern at ABB US Corporate Research Center, Raleigh, North Carolina in 2018. From 2019 to 2021, he was serving as a Product Application Engineer at Automotive Group, Infineon Technologies Americas Corp, El Segundo, California, USA. He has supported multiple Tier 1 suppliers and OEMs. In 2021, he returned to China and joined Hefei University of Technology. He is also serving as a senior researcher at Hefei Comprehensive National Scientific Center, Hefei, China. His research interests include wide bandgap devices modeling, gate driving and applications. He has published over 30 peer-review papers, holds 2 US patents and 6 pending China patents. He is serving as an editor and a reviewer for multiple journals and a session chair for ECCE and APEC. He is a recipient of 2018 IEEE APEC Outstanding Presentation Award. He is a member of IEEE PELS TC2, IAS PEDCC, Eta Kappa Nu and a Senior Member of China Electrotechnical Society

About HFUT and the Team

Hefei: An Innovation Center of China

HFUT: Hefei University of Technology

Hefei Comprehensive National Science Center

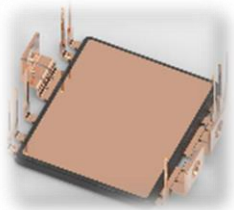
Packaging Lab

power semiconductor packaging: wire-bonding, soldering, Ag-sintering, Gel-filling, plasma-cleaning, etc.

Reliability Lab

HTRB, HTGB, H3TRB, power cycling, thermal shock, salt mist, SAM, X-Ray, and other inspection tools.

- **All about power semiconductor:**
- Packaging
- Aging & Testing
- Gate Driving & Modeling
- Applications: ATV, PV, ESS, Grid…



Seminar Schedule

- 40 mins Parallel connection of SiC MOSFETs in Multichip Power Modules
- 40 mins Active current sharing methodologies

Part I - Parallel Connection of SiC MOSFETs

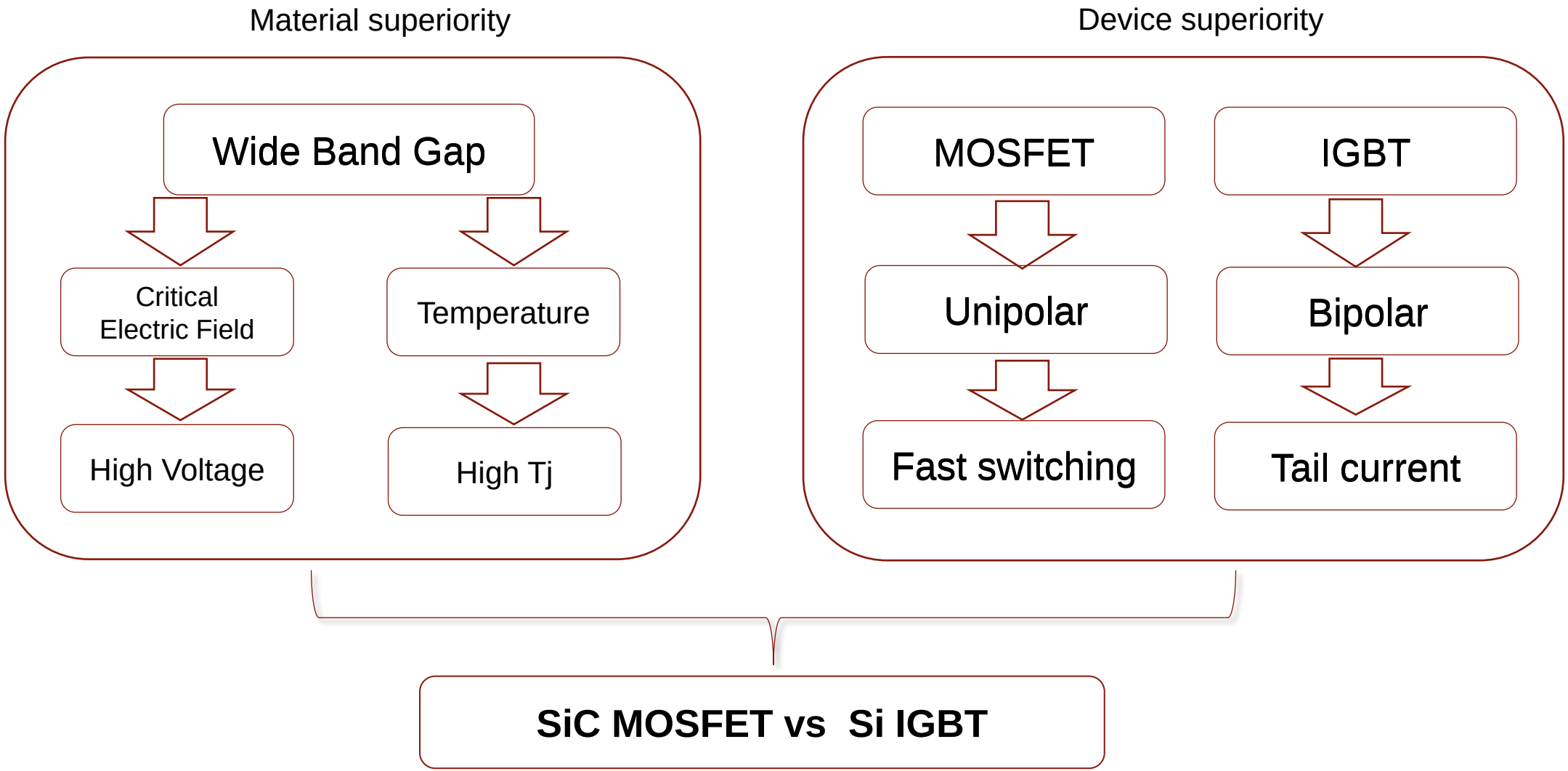
- Status and Challenges of Paralleling SiC MOSFETs
- Current Distribution among Paralleled Devices
  - Influence of device and circuit parameters mismatches
  - Paralleling dies and paralleling half bridges
  - Essence of current imbalance
- Optimization of Multichip Power Module Layout

Part I - Parallel Connection of SiC MOSFETs

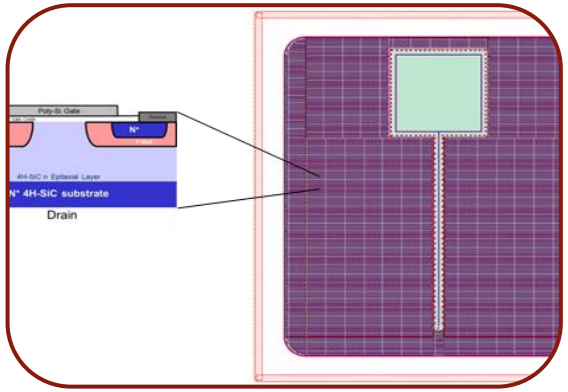
01

Status and Challenges

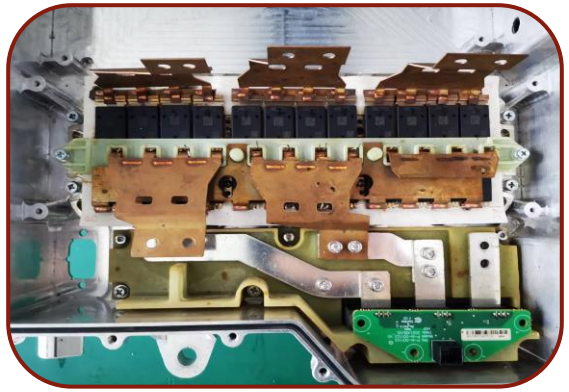
SiC MOSFET vs Si IGBT



Parallel Connection of Silicon Carbide MOSFETs

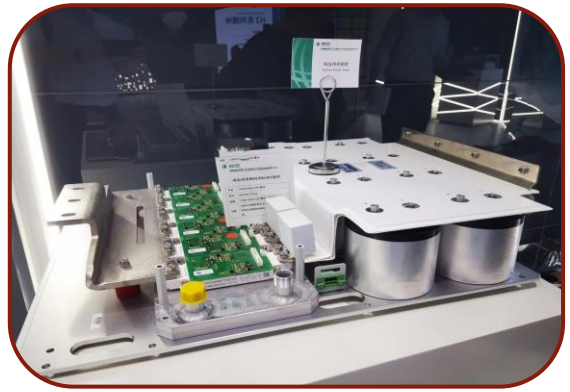


Parallel Unit Cells



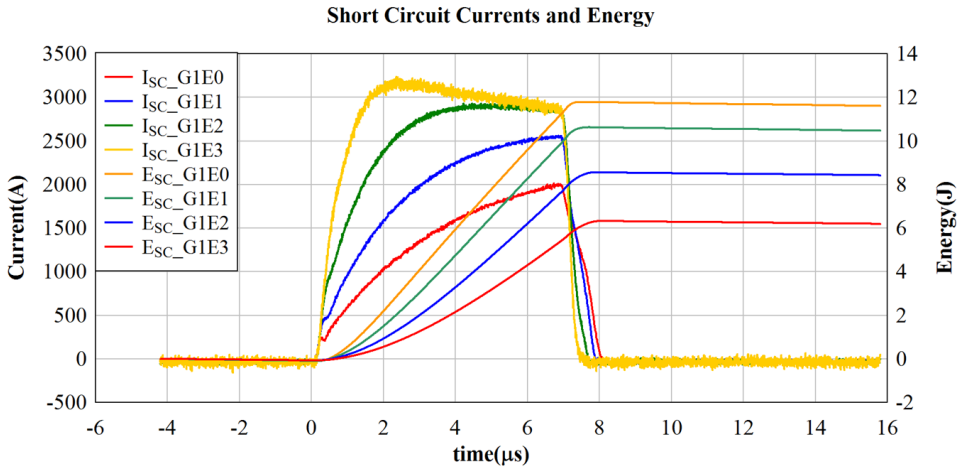
Parallel Discrete Devices

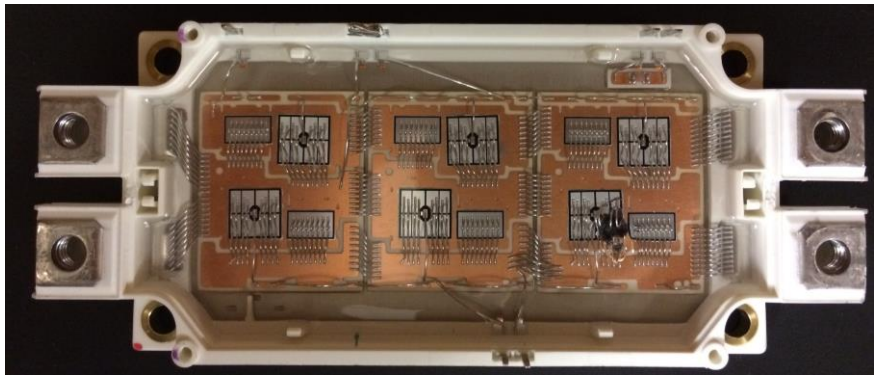
Parallel Bare Dies

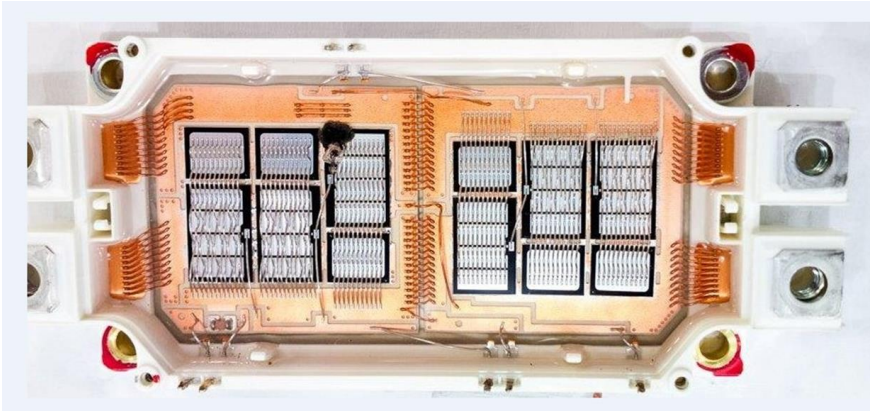


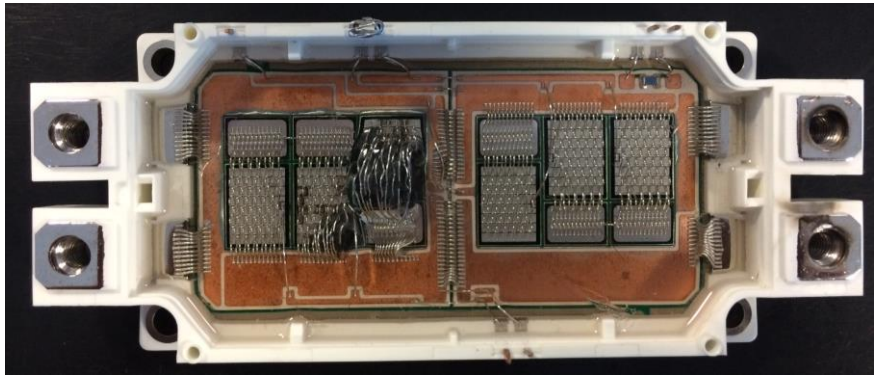
Parallel Power modules

Device failures with paralleled chips





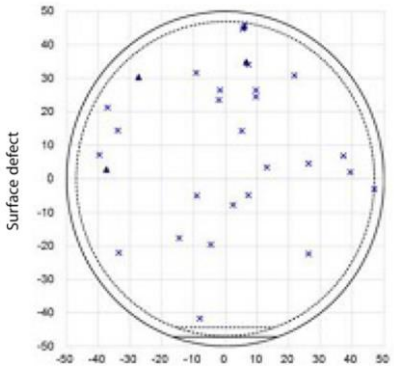




Over current and short circuit current device failures always at the same position

Challenges of Paralleling SiC MOSFETs

Si-IGBT

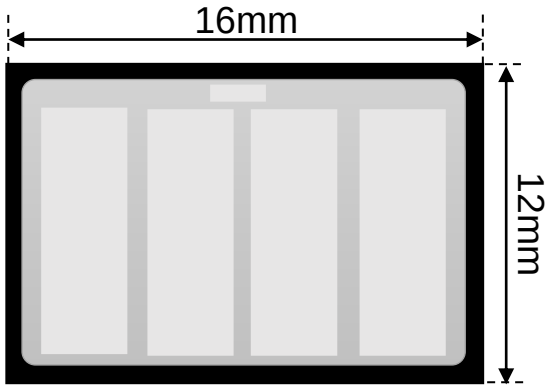


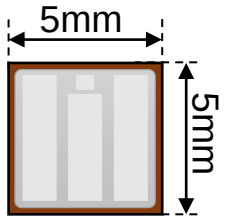
SiC-MOSFET

- 0 defect
- High mature process
- 8 or 12 inch
- >99% yield
- Large chip size

- Material defect density
- Less mature process
- 4 or 6 inch
- Low yield
- Small chip size

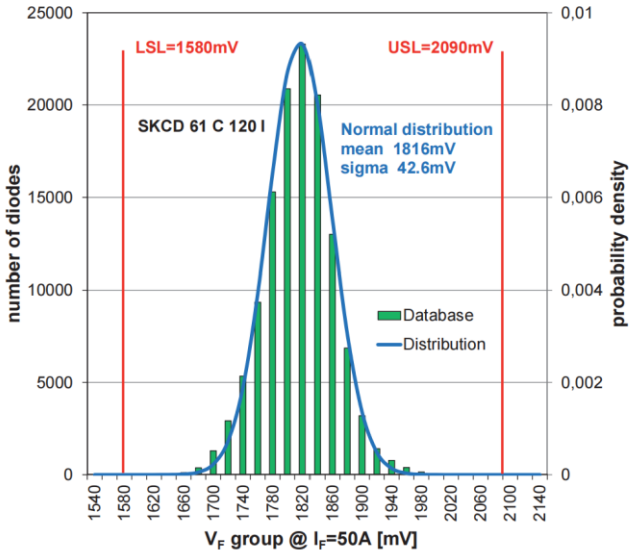
Si IGBT chip
750V
250A-300A





SiC MOSFET chip
750V
80A-120A

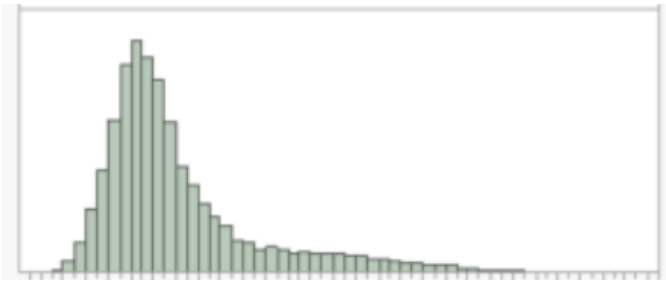
Challenges of Paralleling SiC MOSFETs



Device Parameter Distribution

Si Devices

Narrow and normal distribution

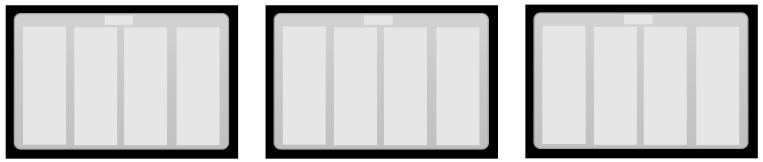


Device Parameter Distribution

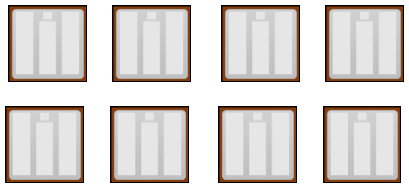
SiC Devices

Wide and “wired” distribution

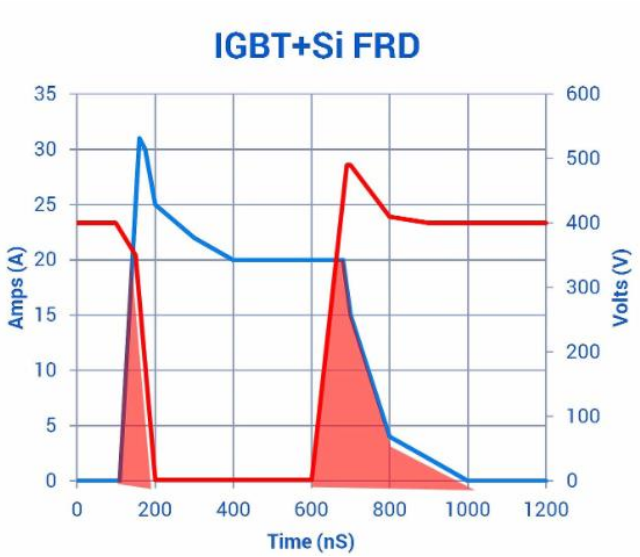
Challenges of Paralleling SiC MOSFETs

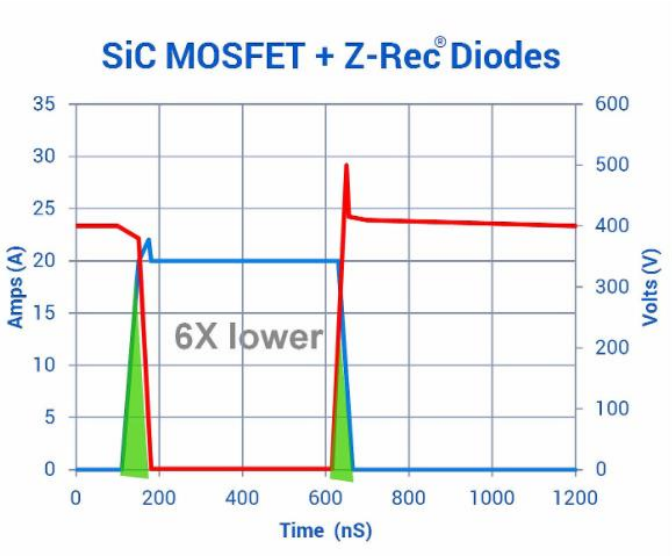


3 x Si IGBT



8 x SiC MOSFETs



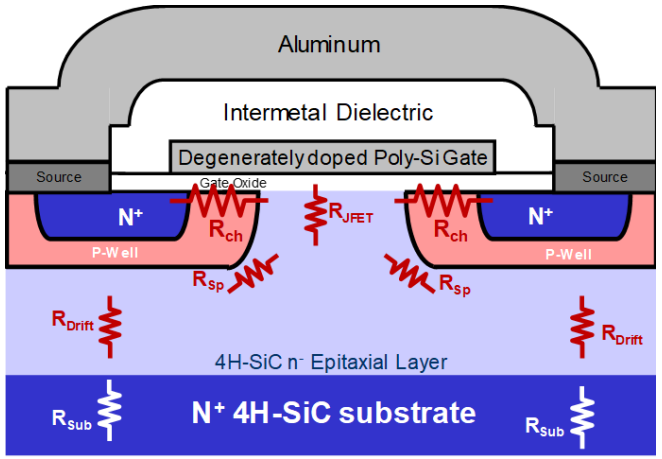


More chips to parallel

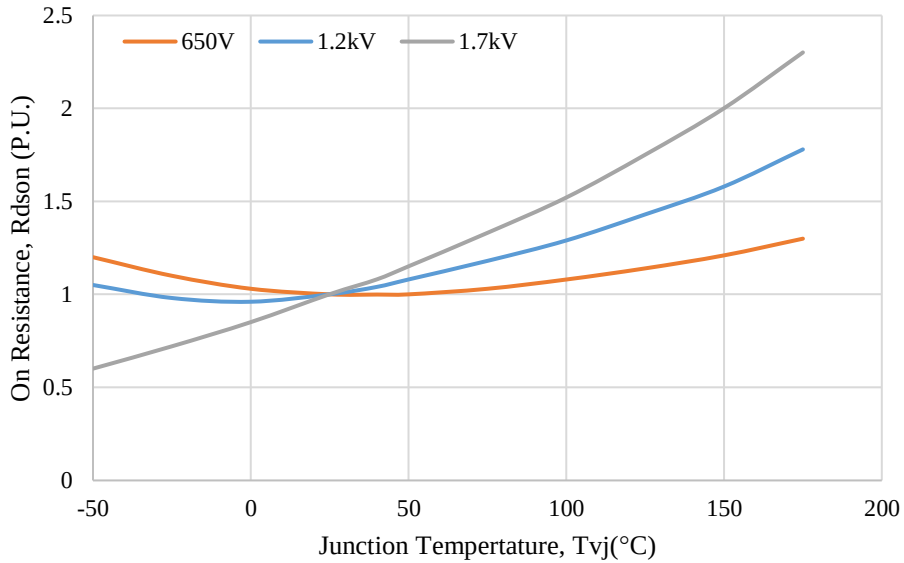
Faster switching speed

Positive temperature coefficient

$R_{dson}=R_{ch}+R_{drift}+R_{contact}+R_{sub}$



Self-Balancing due to positive temperature coefficient



Design Trade-off

Ration of (Rdson vs Tj)

- Higher ratio means more loss but easy for parallel connection
- Lower ratio means less loss but difficult for parallel connection

Higher voltage device has higher ratio of (Rdson vs Tj)

Due to:

- Rdrift have positive temperature coefficient
- Rch have negative temperature coefficient

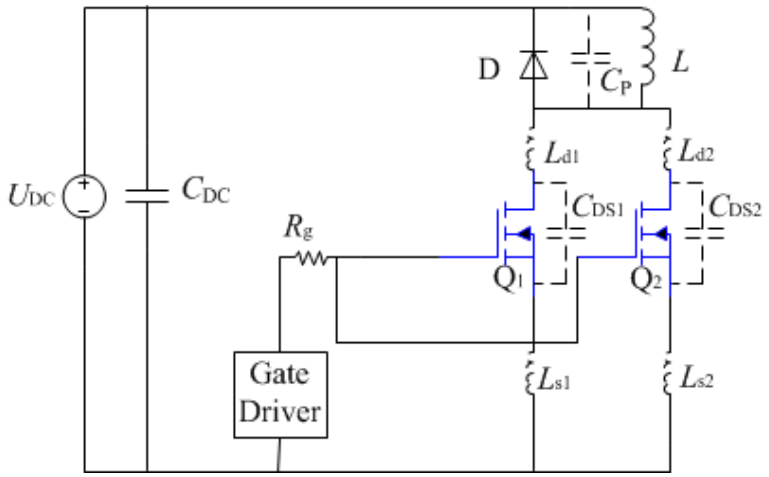
Part I - Parallel Connection of SiC MOSFETs

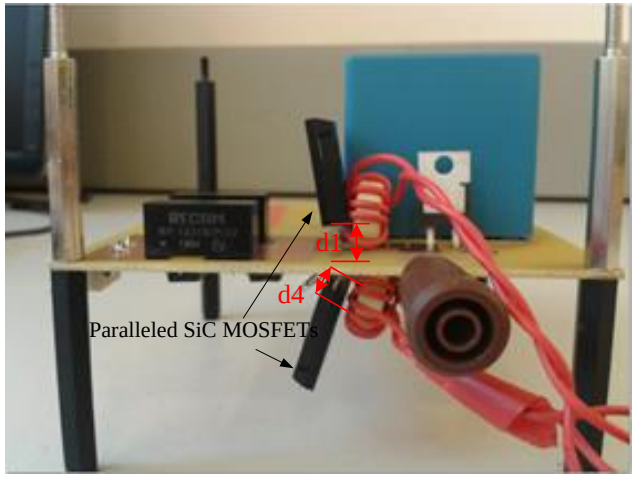
02

Current Distribution

Mechanism of Current Imbalance

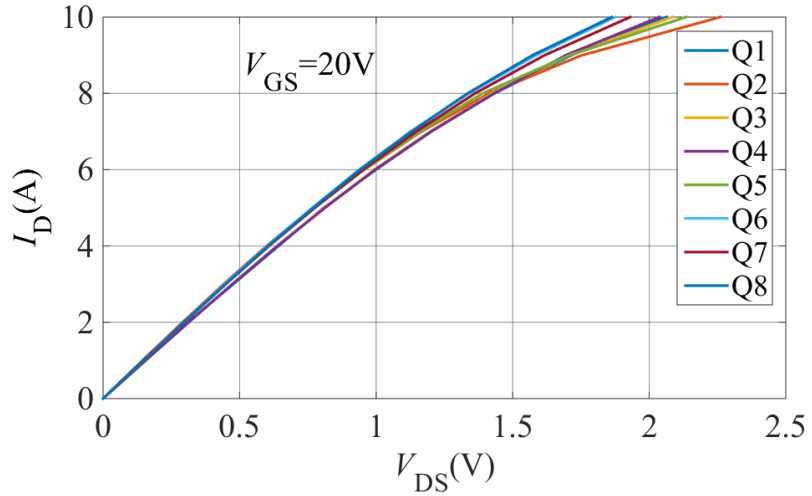
- Device parameters mismatch
  - Influence of R_{on} mismatch
  - Influence of V_{th} mismatch
- Circuit parameters mismatch
  - Influence of L_d mismatch
  - Influence of L_s mismatch



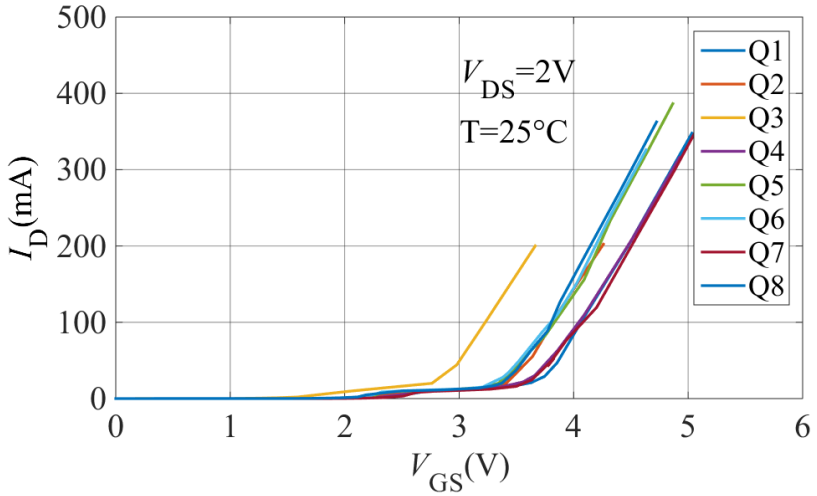


- Symmetric layout design
- Easy to adjust circuit mismatch
- Good for benchmarking

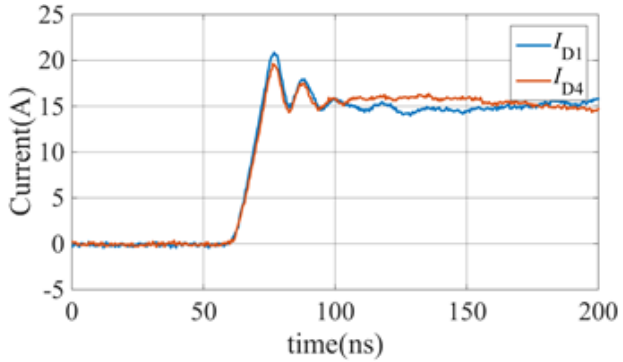
Current distribution

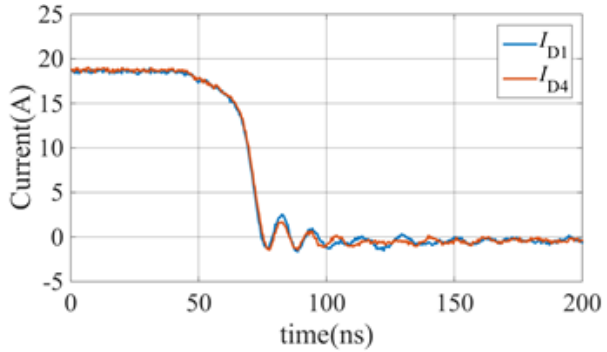


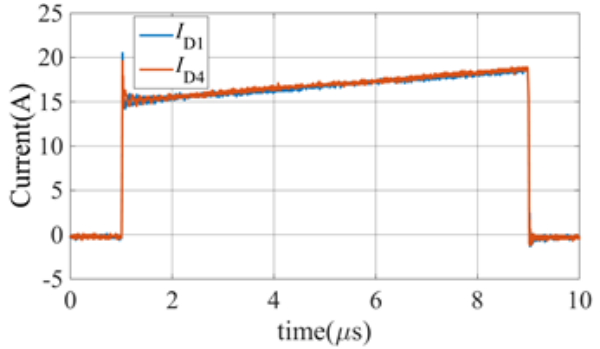
Devices output characterization



Devices transfer characterization



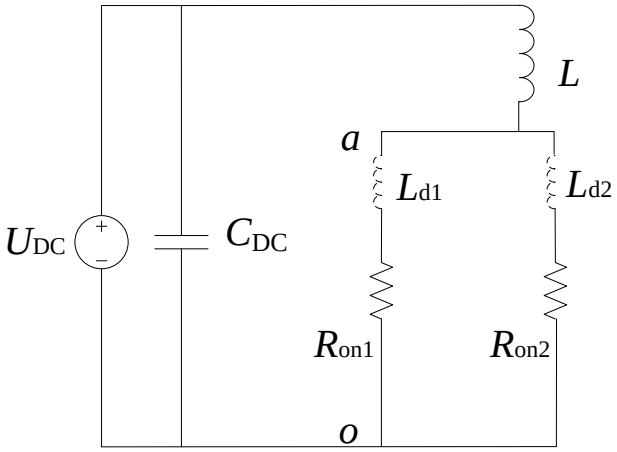


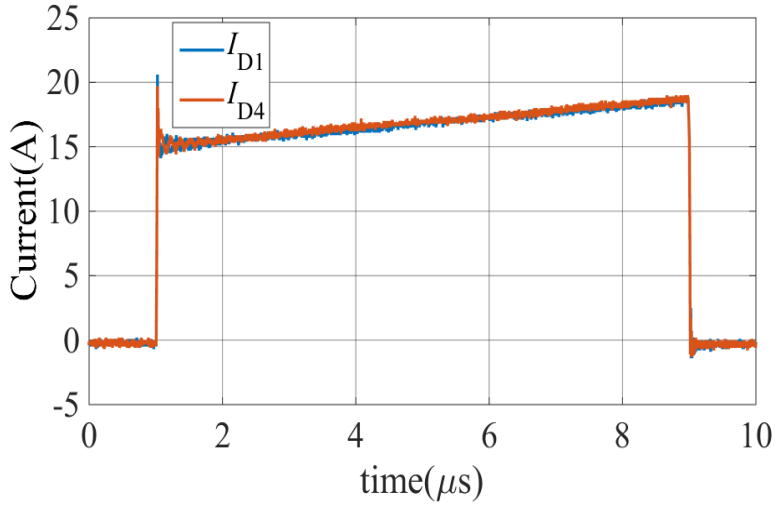


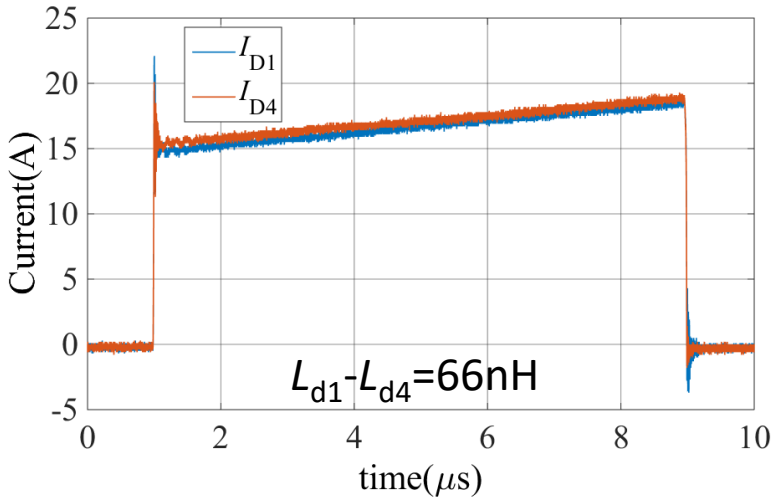
Benchmarking

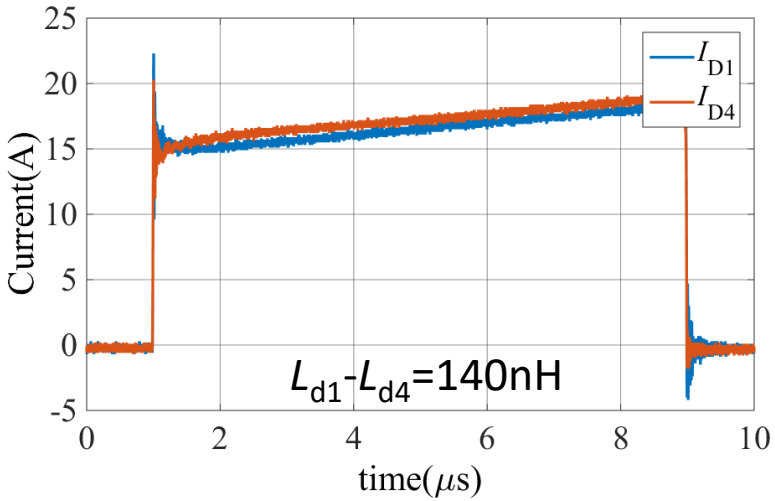
Current distribution without device parameters' mismatch and without circuit parameters' mismatch

Current distribution with L_d mismatch

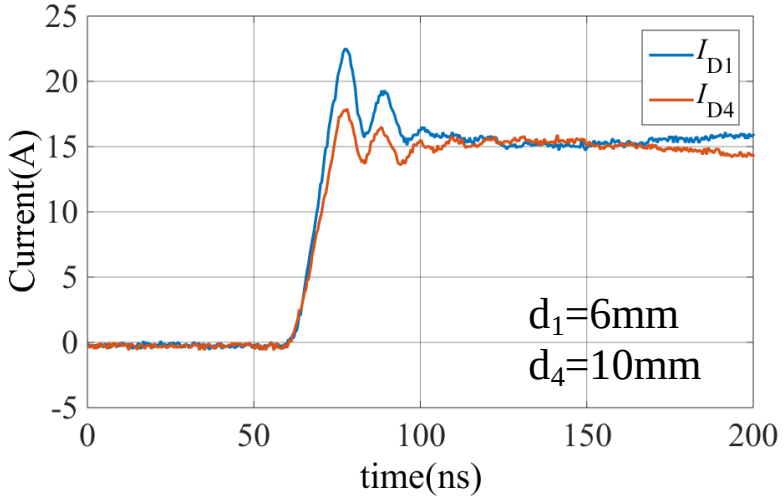


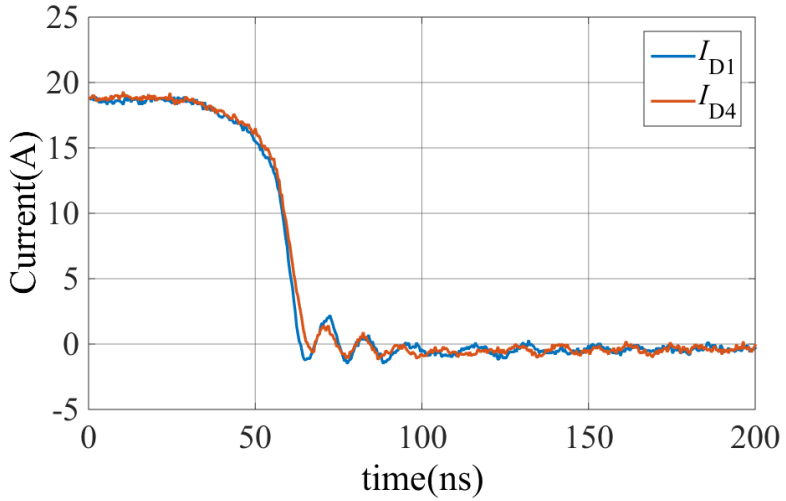


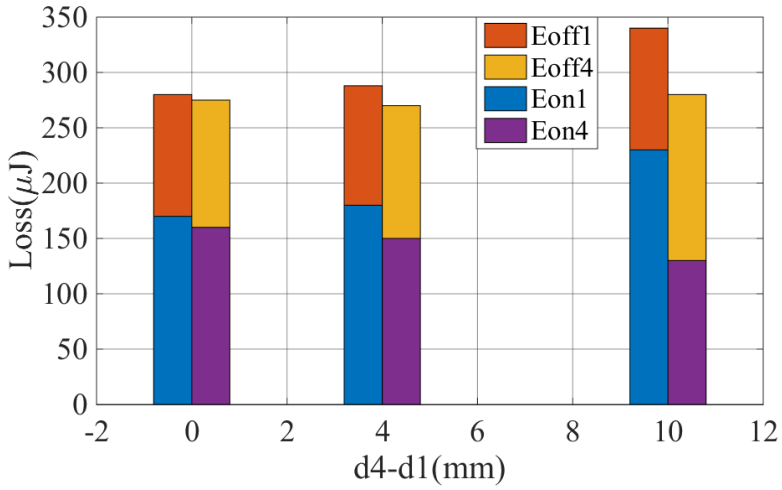


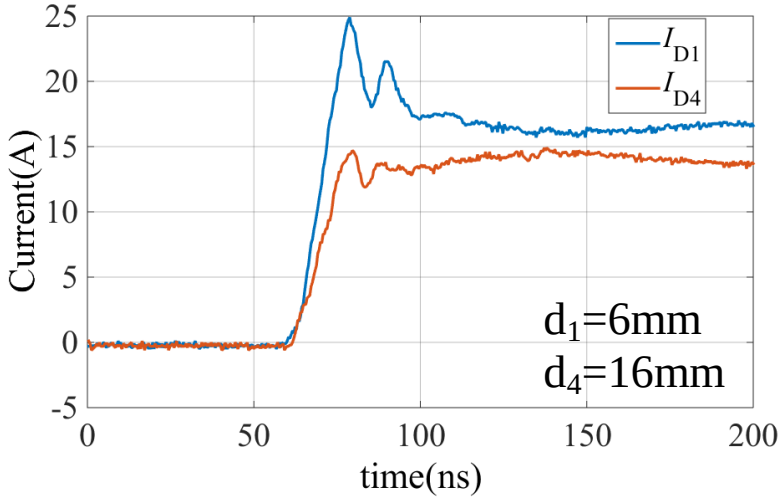


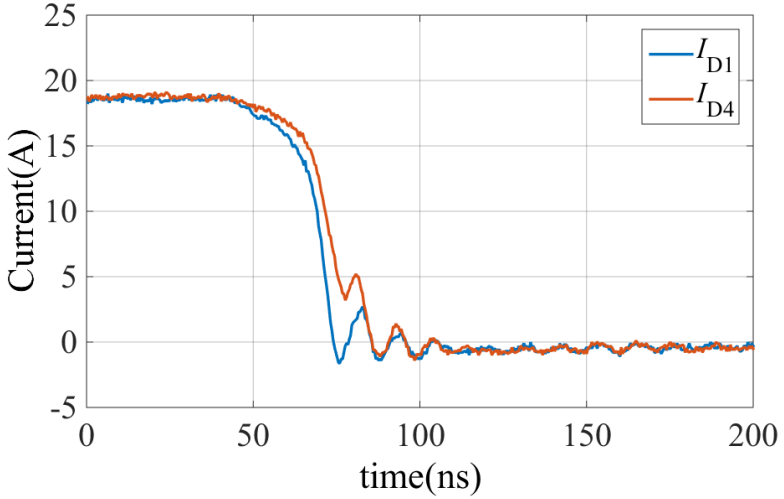
Current distribution with *L*s mismatch





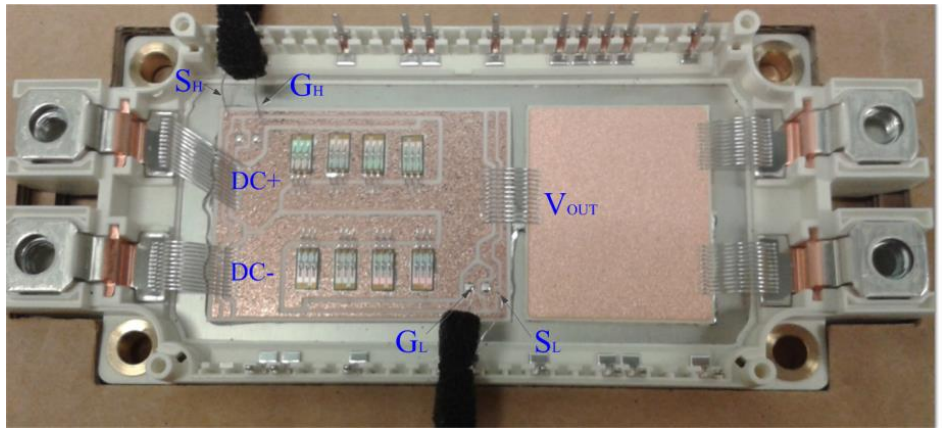




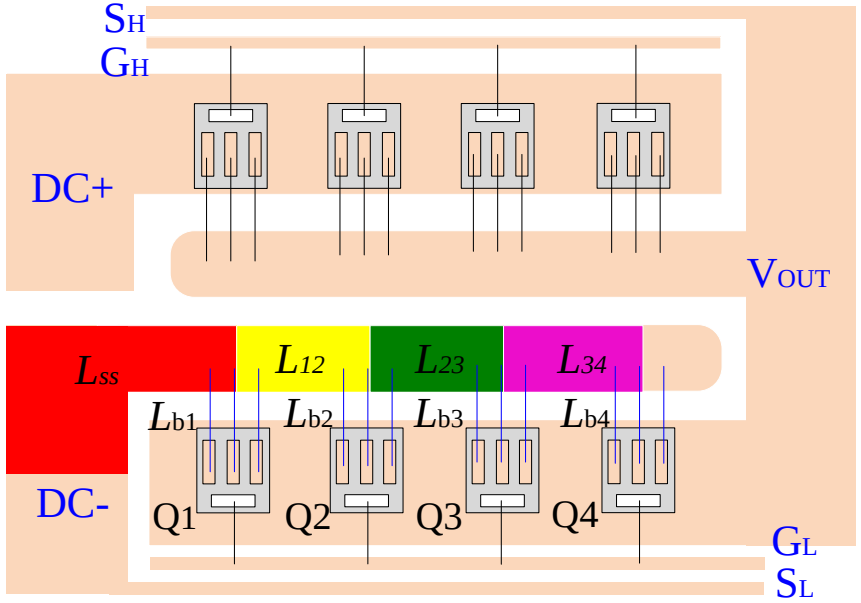


- L_s mismatch leads to transient current imbalance.
- Larger L_s leads to a smaller device turn-on current and smaller turn-on loss, while it leads to a slower turn-off current and larger turn-off loss.
- For parallel connection, larger L_s cause smaller device power losses. This is different with the effect of L_s for a single device.

Multichip power modules layout

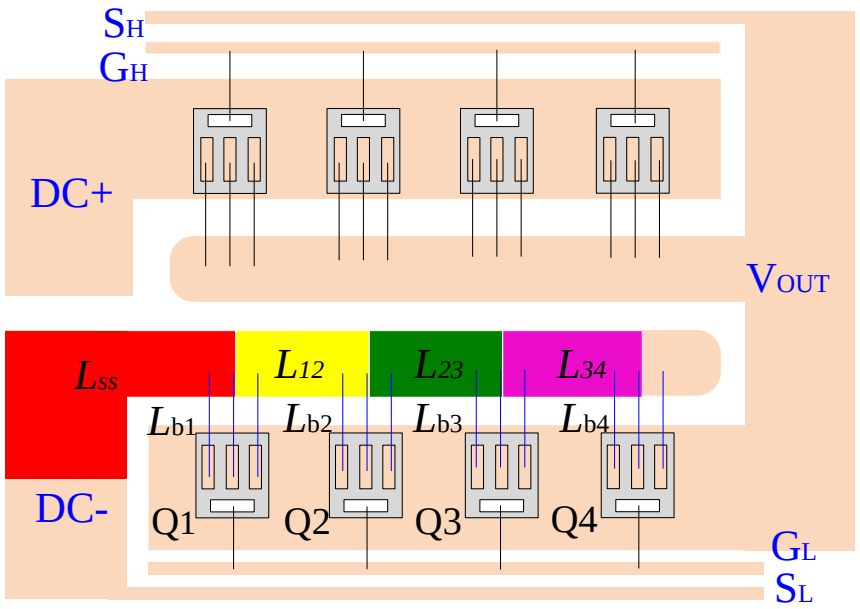


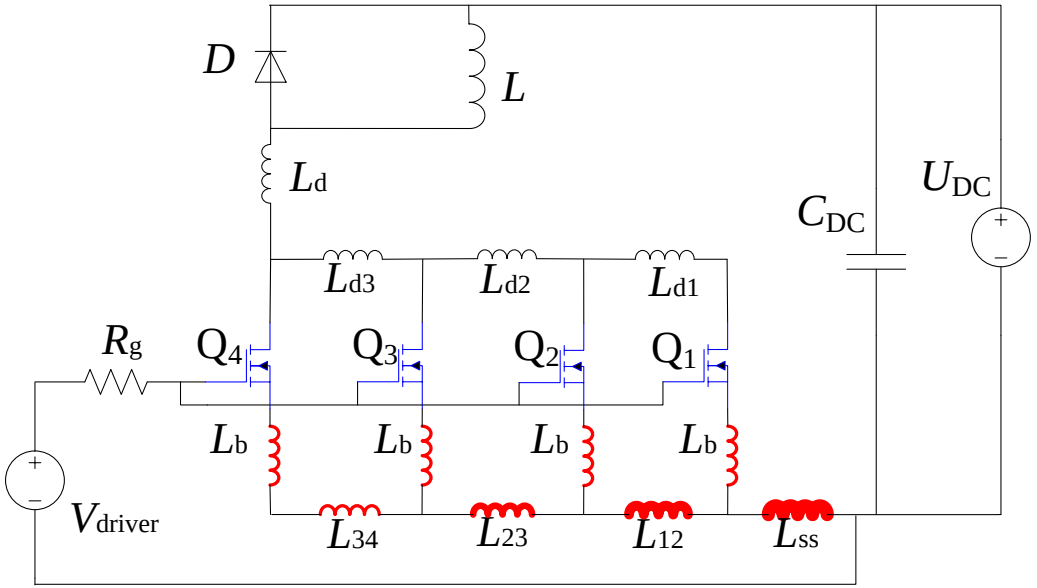
Customized 1.7kV/200A power module



Power module layout

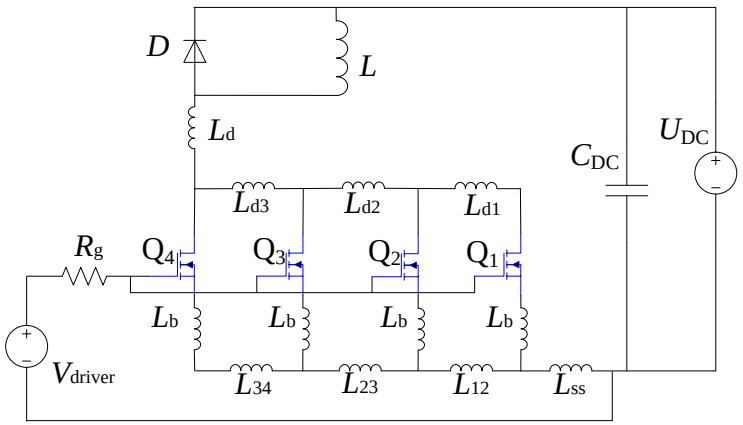
Modeling of multichip power modules layout

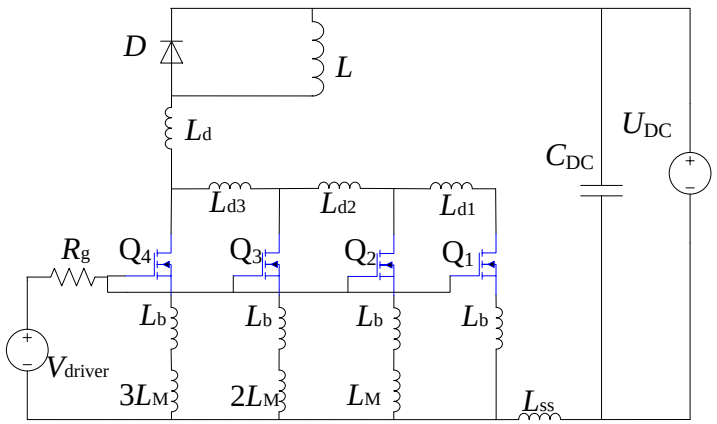




Mismatch of L_s

Current coupling effects





$$\begin{cases} L_{s1} = L_{ss} + L_b \\ L_{s2} = L_{ss} + L_{12} + L_b = L_{ss} + L_{\mathrm{M}} + L_b \\ L_{s3} = L_{ss} + L_{12} + L_{23} + L_b = L_{ss} + 2L_{\mathrm{M}} + L_b \\ L_{s4} = L_{ss} + L_{12} + L_{23} + L_{34} + L_b = L_{ss} + 3L_{\mathrm{M}} + L_b \end{cases}$$

$$L\frac{\mathrm{d}i}{\mathrm{d}t}$$

Identical mismatch value of *Ls*

Difference

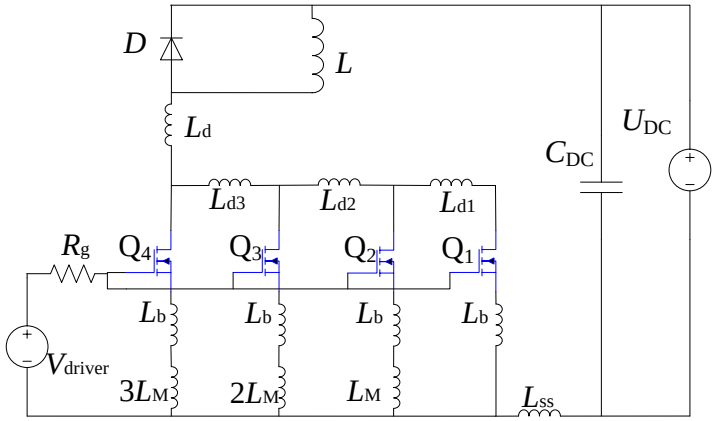
Current Coupling Effect:

- The current on the mismatched Ls is not only from one device.
- The current of one device is not only affected by its own current but also the paralleled other devices.
- It is the mismatched Ls*di/dt which affects VGS and therefore affects the transient current distribution.

H. Li, S. Munk-Nielsen, S. Beczkowski, R. Maheshwari, T. Franke, 'Circuit mismatch and current coupling effect on paralleling SiC MOSFETs in multichip power modules', PCIM Europe 2015, Germany. (Nominated Young Engineer Award)

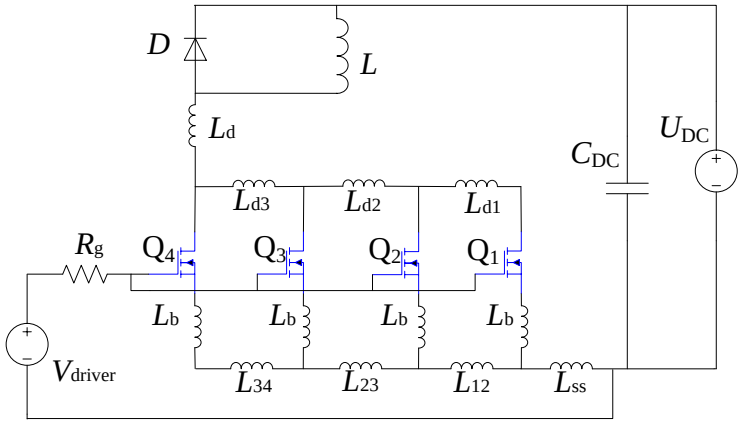
Current coupling effects

$$\begin{cases} i_{D1}-i_{D2}=g_{fs}(\triangle V_{LS2}-\triangle V_{LS1})=g_{fs}\left[L_b\dfrac{d(i_{D2}-i_{D1})}{dt}+L_{12}\dfrac{di_{D2}}{dt}\right] \\ i_{D2}-i_{D3}=g_{fs}(\triangle V_{LS3}-\triangle V_{LS2})=g_{fs}\left[L_b\dfrac{d(i_{D3}-i_{D2})}{dt}+L_{23}\dfrac{di_{D3}}{dt}\right] \\ i_{D3}-i_{D4}=g_{fs}(\triangle V_{LS4}-\triangle V_{LS3})=g_{fs}\left[L_b\dfrac{d(i_{D4}-i_{D3})}{dt}+L_{34}\dfrac{di_{D4}}{dt}\right] \\ i_{D1}-i_{D4}=g_{fs}(\triangle V_{LS4}-\triangle V_{LS1})=g_{fs}\left[L_b\dfrac{d(i_{D4}-i_{D1})}{dt}+(L_{12}+L_{23}+L_{34})\dfrac{di_{D4}}{dt}\right] \end{cases}$$

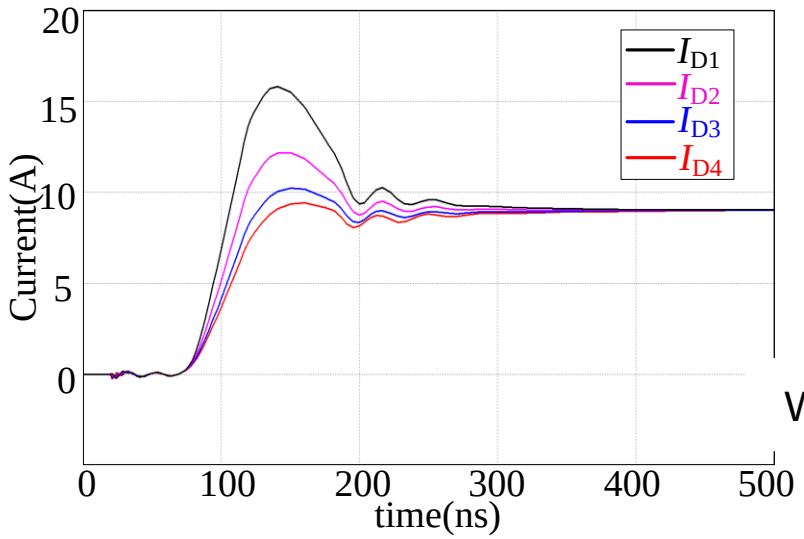


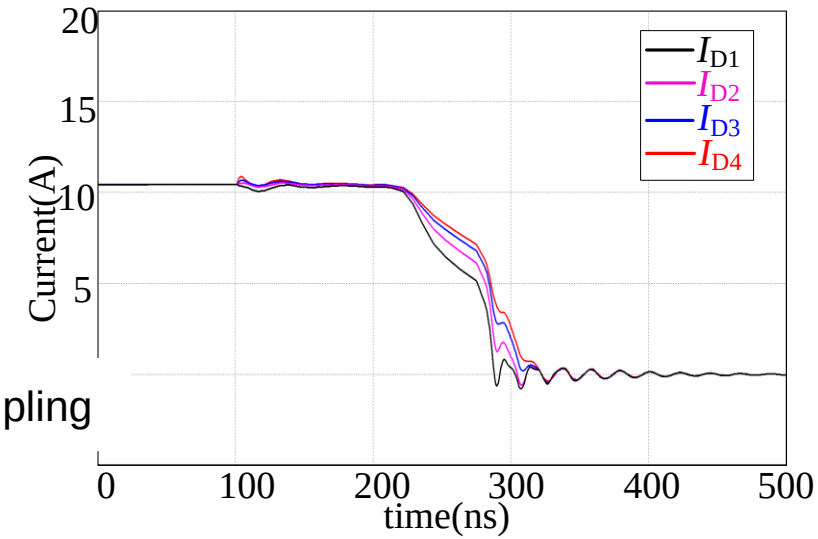
$$\begin{cases} i_{D1}-i_{D2}=g_{fs}(\triangle V_{LS2}-\triangle V_{LS1})=g_{fs}\left[L_b\dfrac{d(i_{D2}-i_{D1})}{dt}+L_{12}\dfrac{di_{D2}}{dt}+L_{12}\dfrac{d(i_{D3}+i_{D4})}{dt}\right] \\ i_{D2}-i_{D3}=g_{fs}(\triangle V_{LS3}-\triangle V_{LS2})=g_{fs}\left[L_b\dfrac{d(i_{D3}-i_{D2})}{dt}+L_{23}\dfrac{di_{D3}}{dt}+L_{23}\dfrac{di_{D4}}{dt}\right] \\ i_{D3}-i_{D4}=g_{fs}(\triangle V_{LS4}-\triangle V_{LS3})=g_{fs}\left[L_b\dfrac{d(i_{D4}-i_{D3})}{dt}+L_{34}\dfrac{di_{D4}}{dt}\right] \\ i_{D1}-i_{D4}=g_{fs}(\triangle V_{LS4}-\triangle V_{LS1})=g_{fs}\left[L_b\dfrac{d(i_{D4}-i_{D1})}{dt}+(L_{12}+L_{23}+L_{34})\dfrac{di_{D4}}{dt}+L_{12}\dfrac{d(i_{D2}+i_{D3})}{dt}+L_{23}\dfrac{di_{D3}}{dt}\right] \end{cases}$$

Current coupling effect

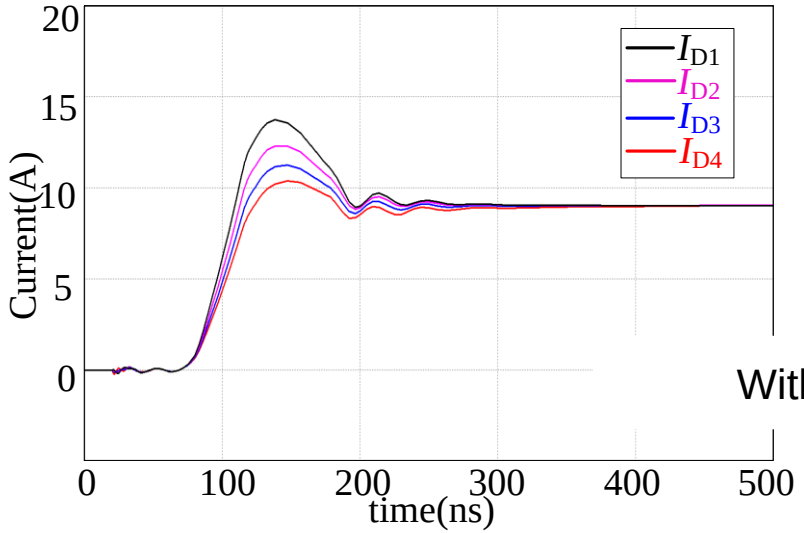


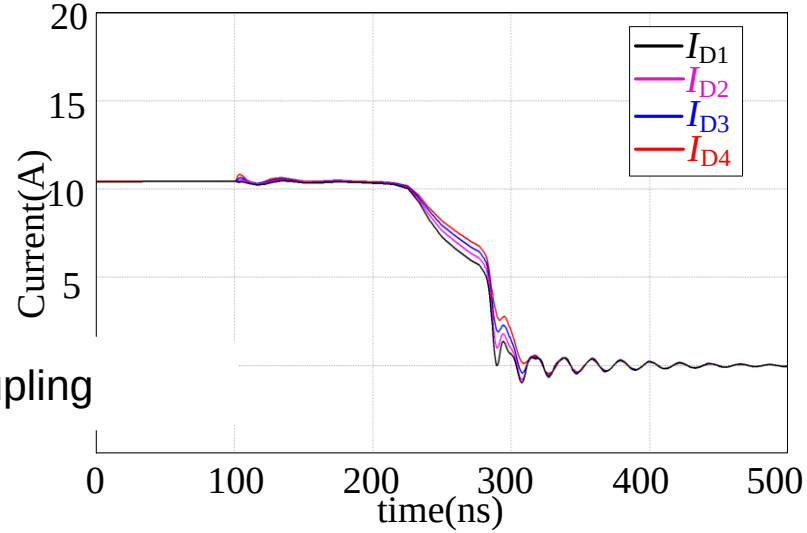
Simulation results





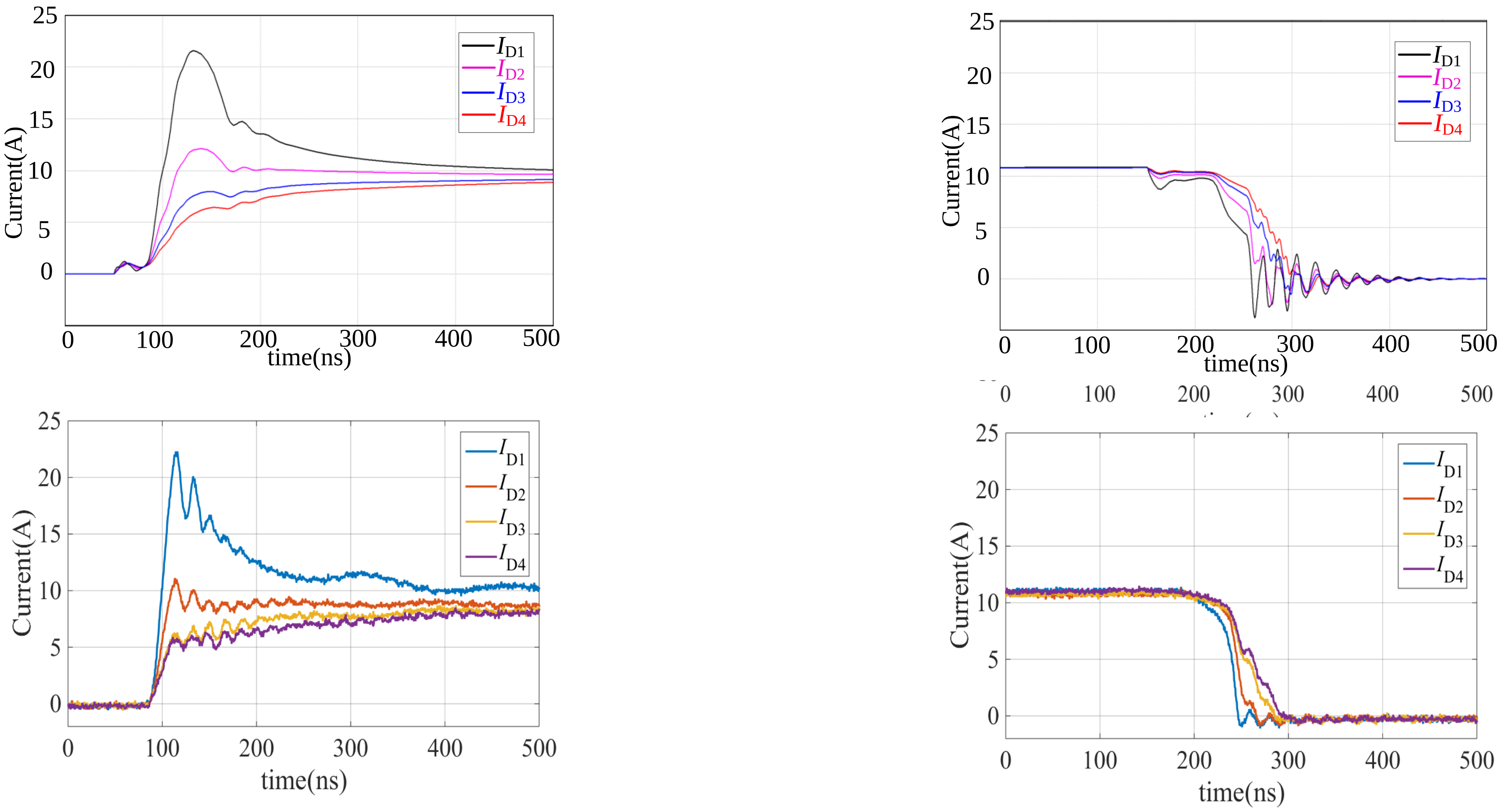
With current coupling





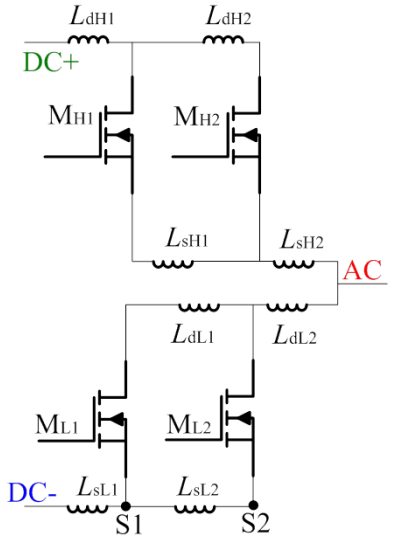
Without current coupling

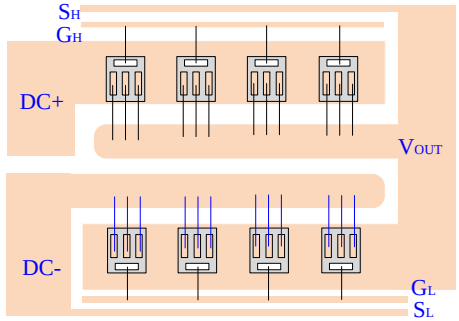
Simulation and Experimental Comparison

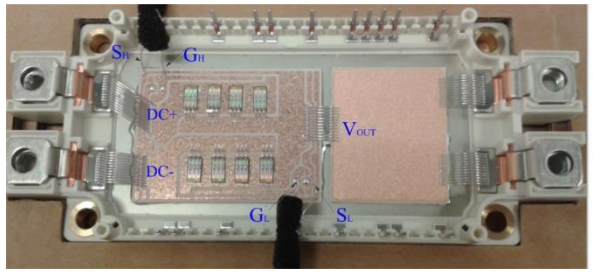


H. Li, S. Munk-Nielsen, X. Wang, R. Maheshwari, S. Beczkowski, C. Uhrenfeldt, Toke Franke, ‘Influences of device and circuit mismatches on paralleling silicon carbide MOSFETs’, *IEEE Transaction on Power Electronics*, Volume 31, issue 1, 2016, Pages: 621 - 634.

Paralleling dies or Paralleling half bridges

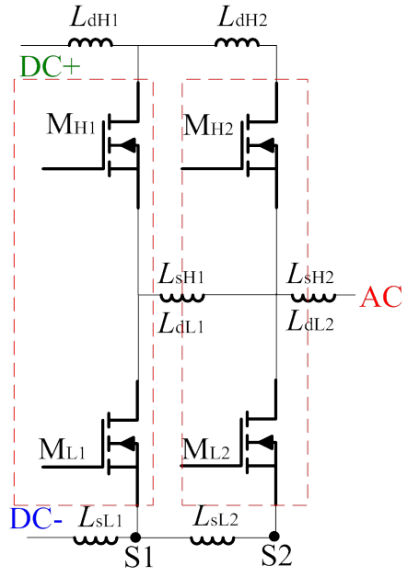


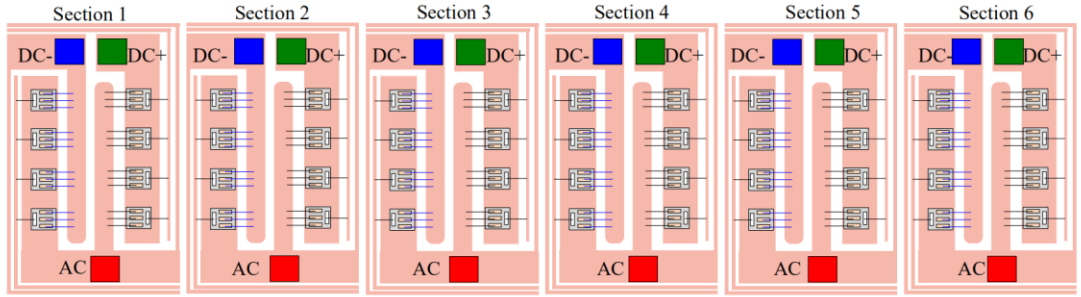




Paralleling dies:

The devices are first paralleled to form a switch and then connected to form a half bridge.

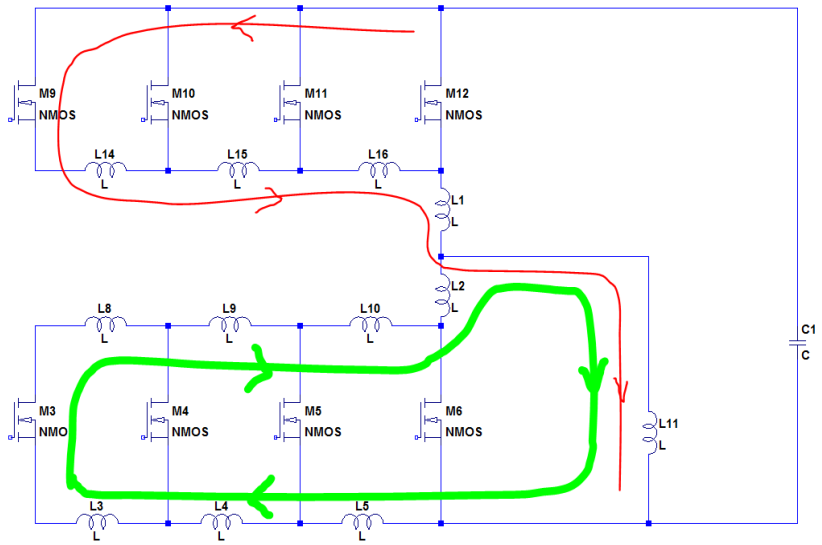


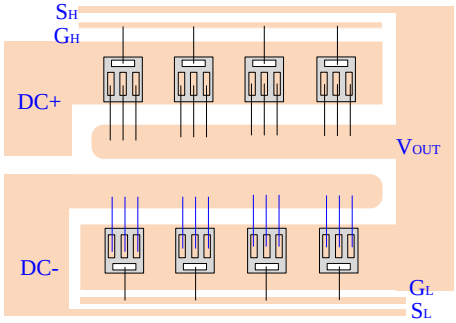


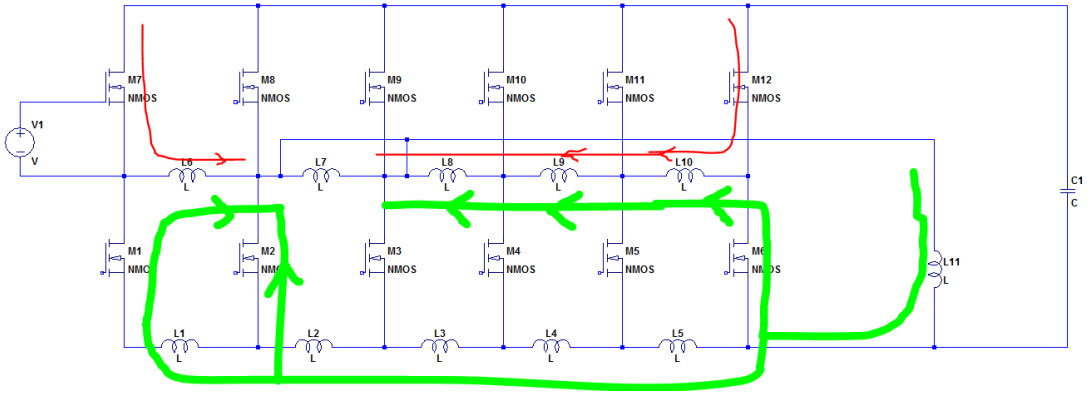
Paralleling half bridges:

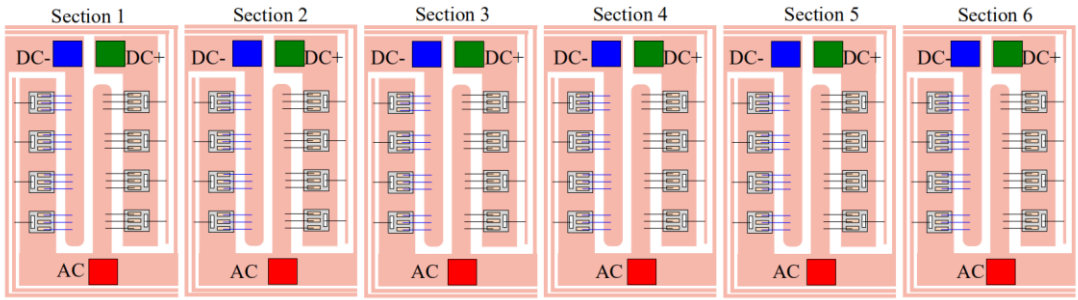
The devices are connected both in parallel and in half bridge configuration. The key is that it can be split into separate half bridges.

Current commutation loop of paralleling dies

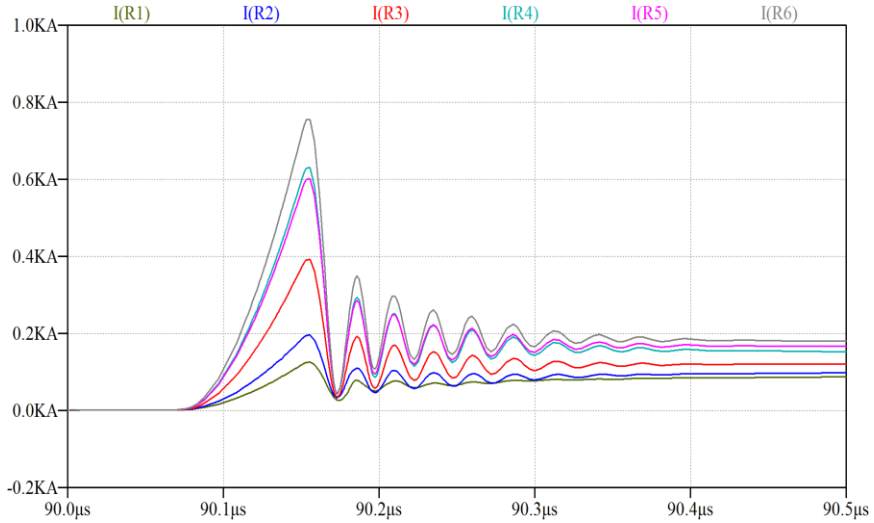


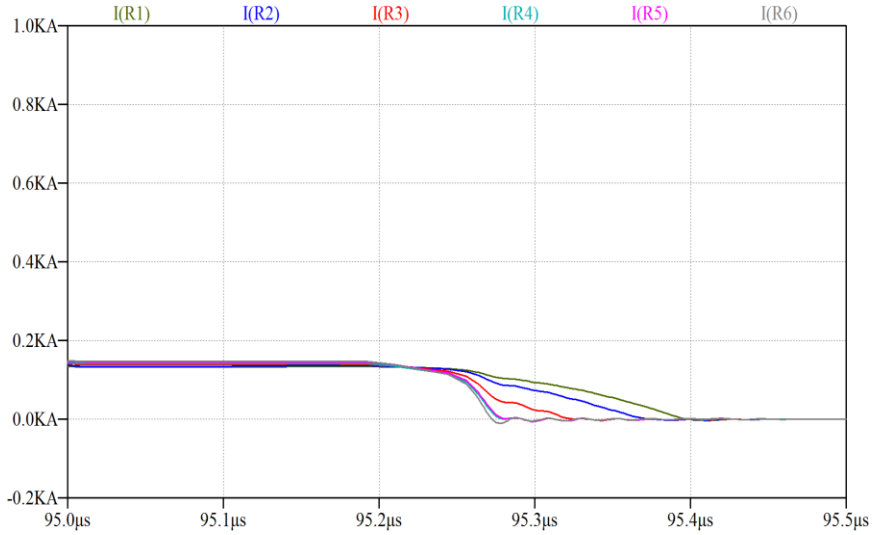




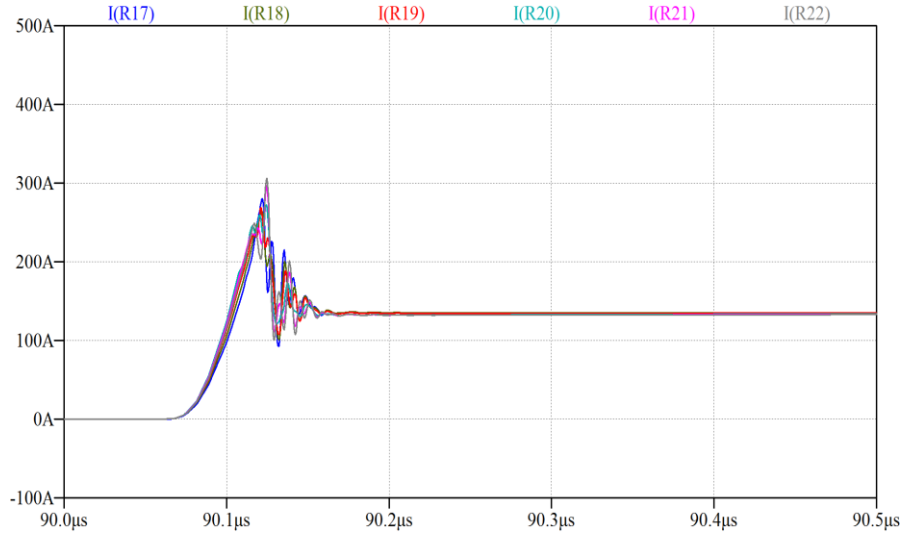


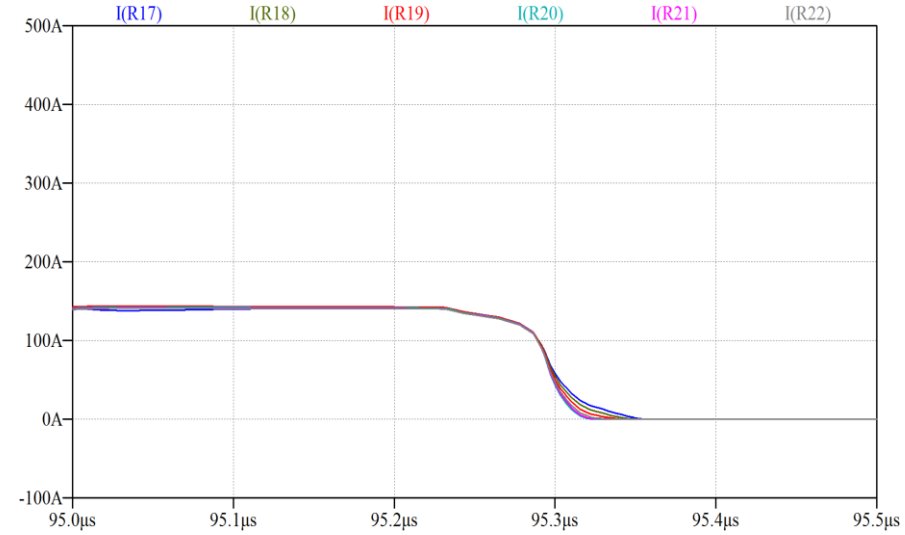
Simulation Results





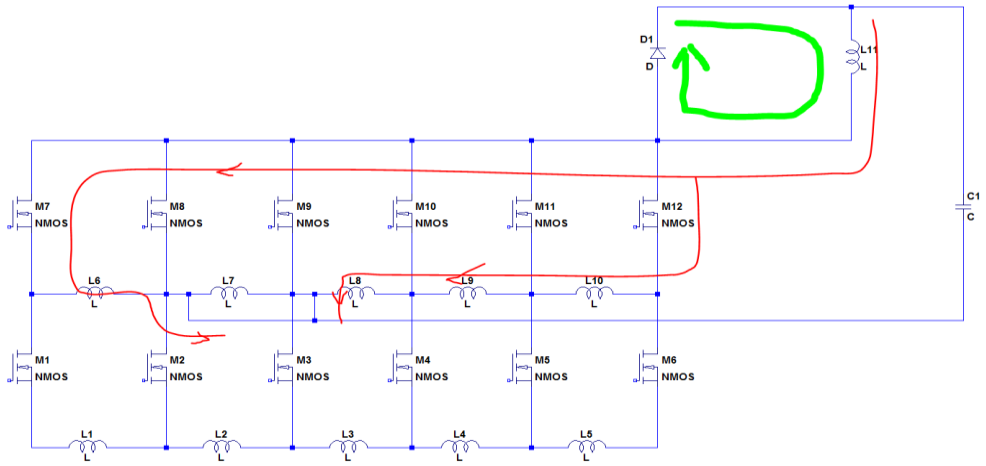
Current distribution among **low side substrates**

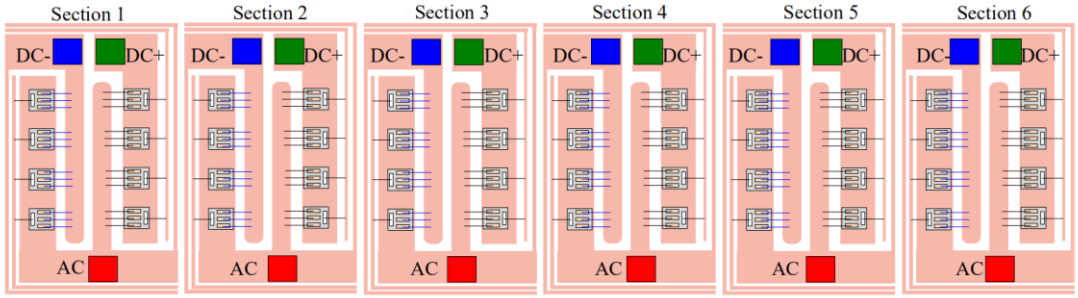


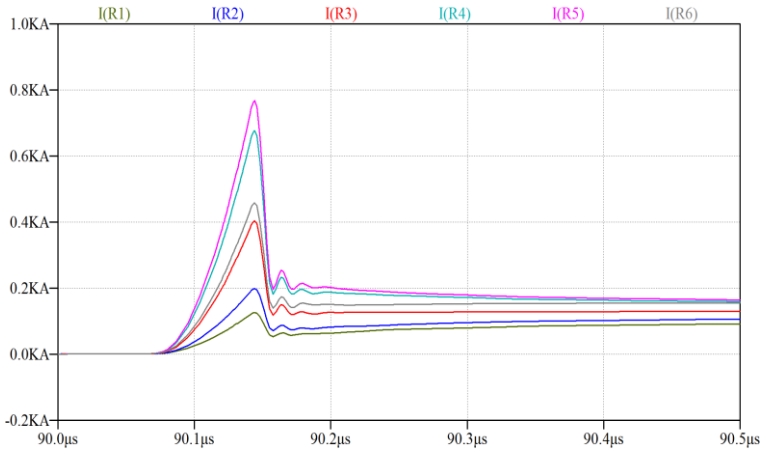


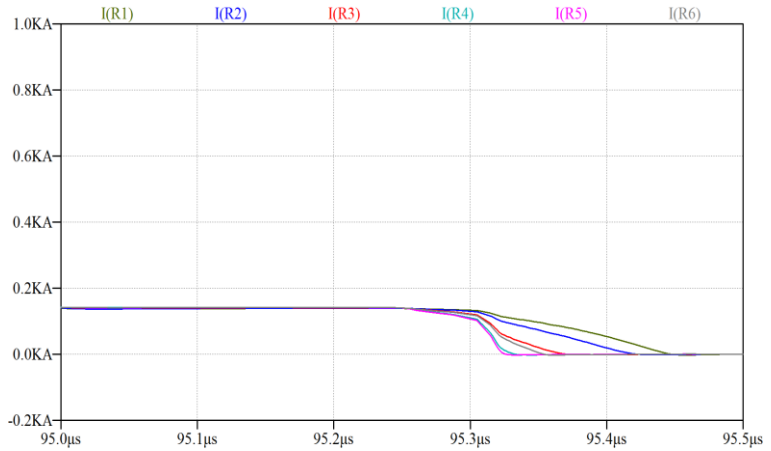
Current distribution among **high side substrates**

Simulation of high side switch in another way







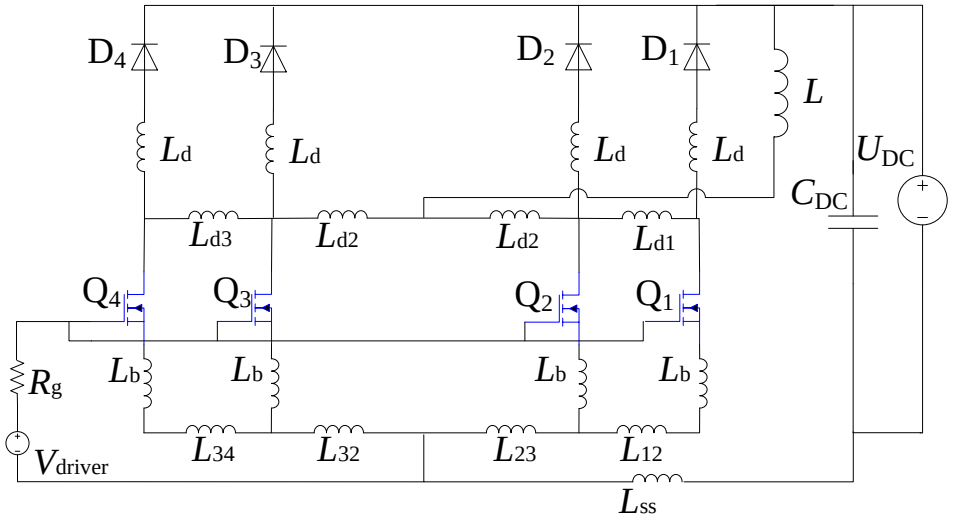


Part I - Parallel Connection of SiC MOSFETs

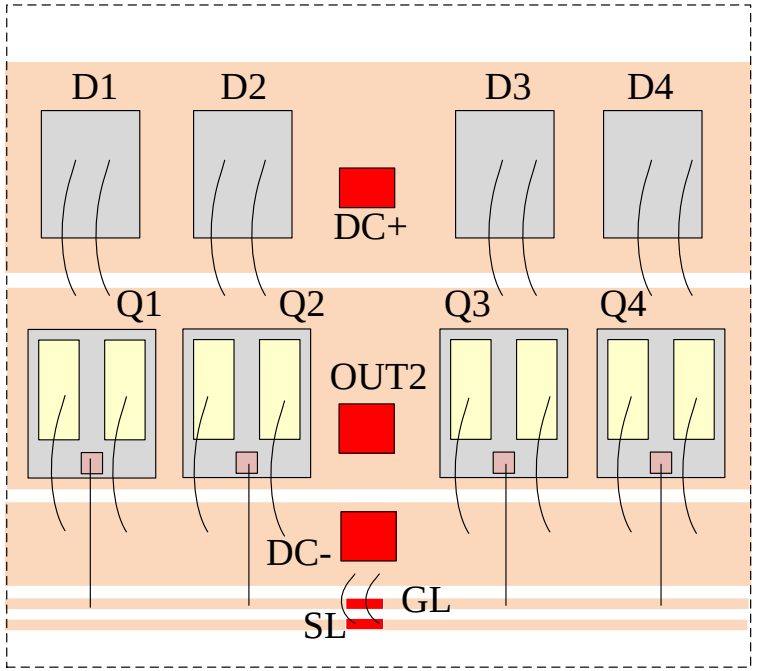
03

Optimization of package layout

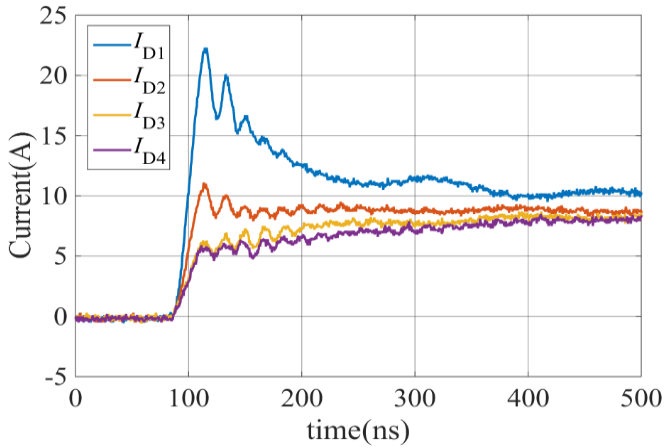
Passive solution: Optimization of package layout

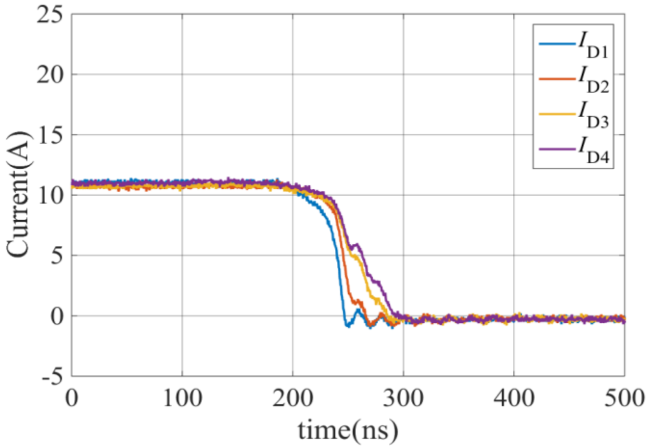


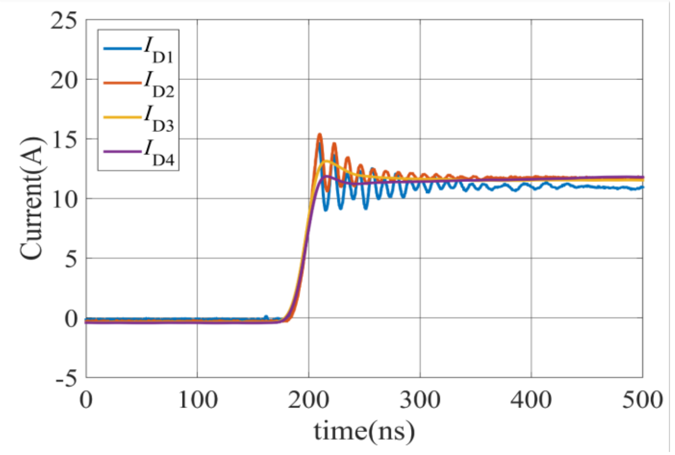
$$\begin{cases} i_{D2}-i_{D1}=g_{fs}\left[L_b\dfrac{d(i_{D1}-i_{D2})}{dt}+L_{12}\dfrac{di_{D1}}{dt}\right] \\ i_{D2}-i_{D3}=0 \\ i_{D3}-i_{D4}=g_{fs}\left[L_b\dfrac{d(i_{D4}-i_{D3})}{dt}+L_{34}\dfrac{di_{D4}}{dt}\right] \\ i_{D1}-i_{D4}=0 \end{cases}$$

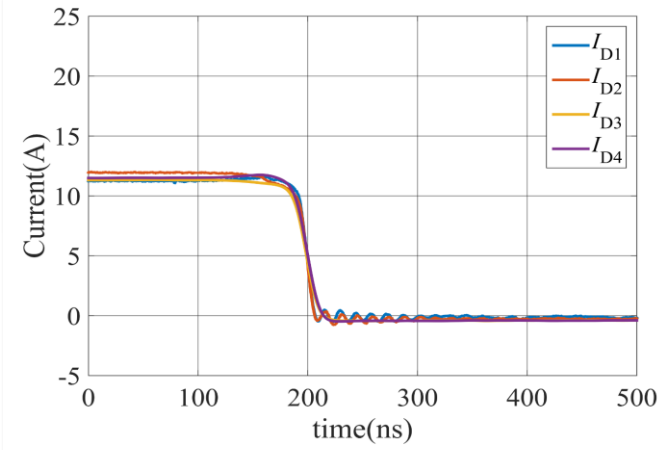


Experimental Results



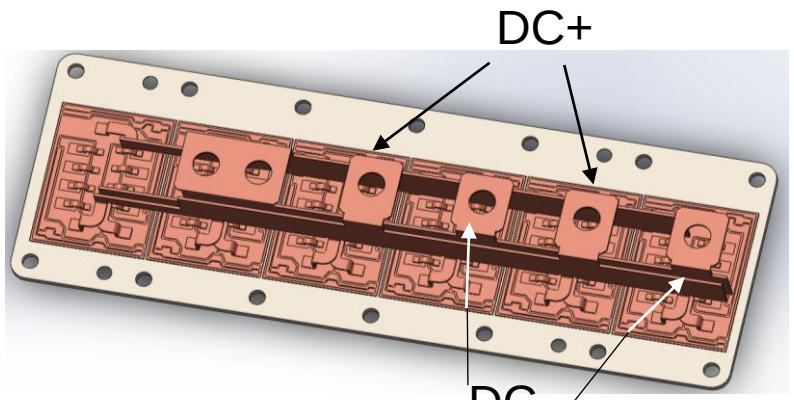


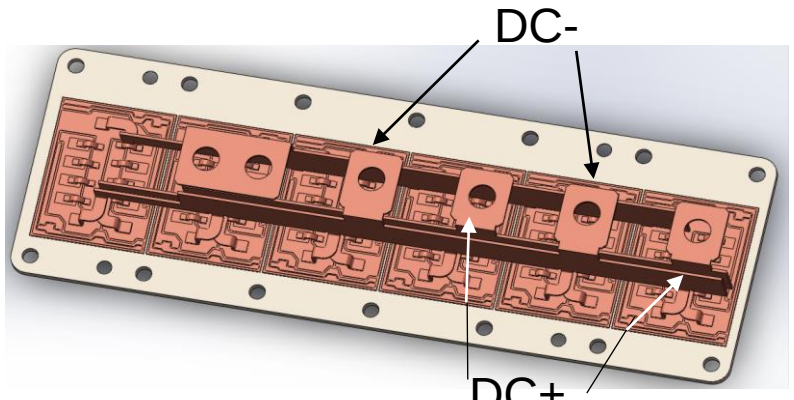


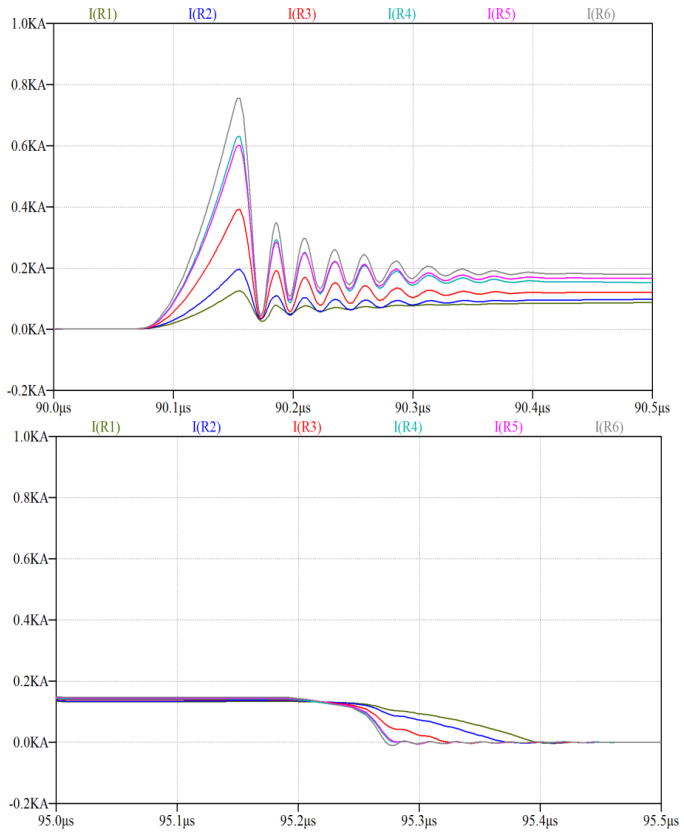


H. Li, S. Munk-Nielsen, S. Beczkowski, X. Wang, ‘A Novel DBC layout for current imbalance mitigation in SiC MOSFET multichip power module’, IEEE Transaction on Power Electronics Letters, 2016

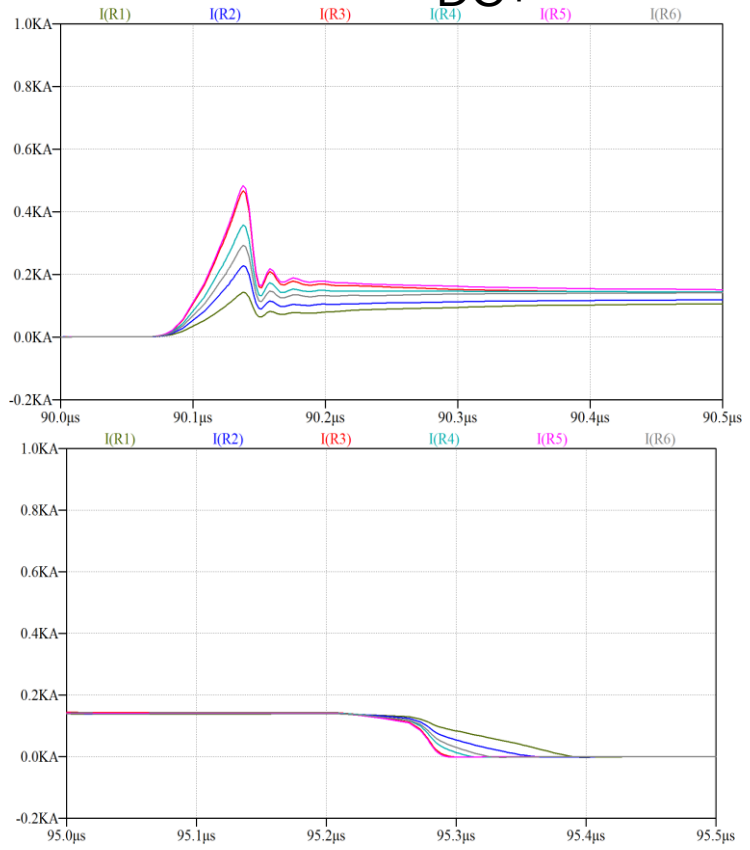
Swap DC+ and DC- screw terminals



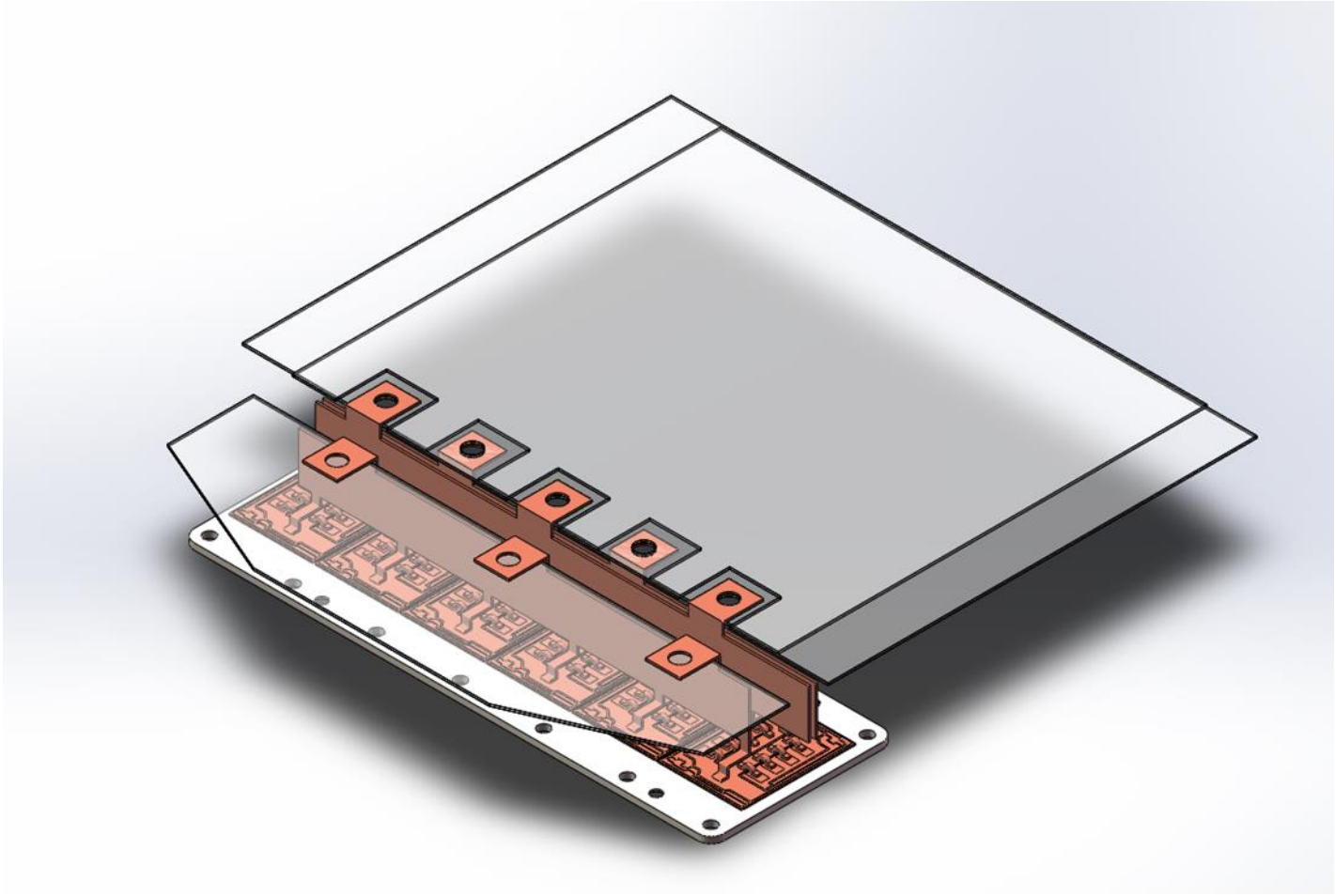




Slightly improved

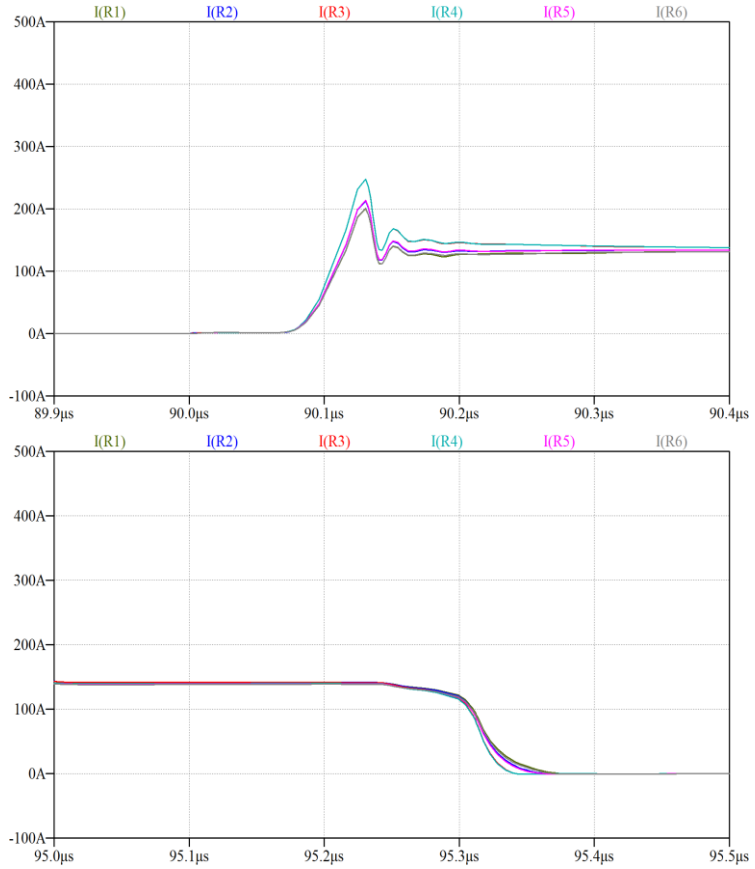


Modified bus bar structure

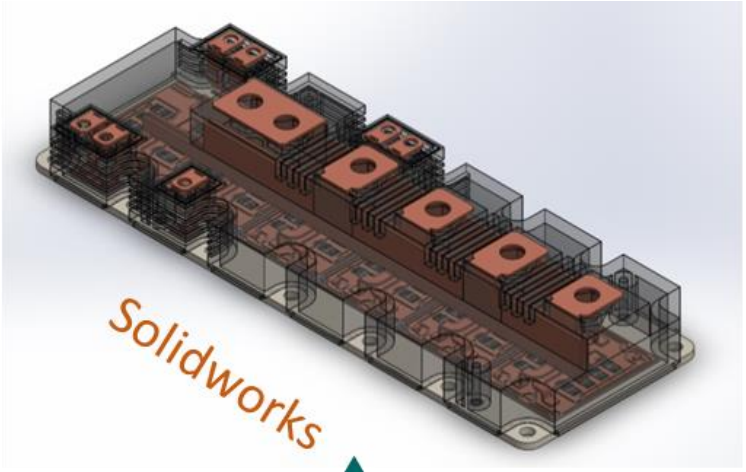


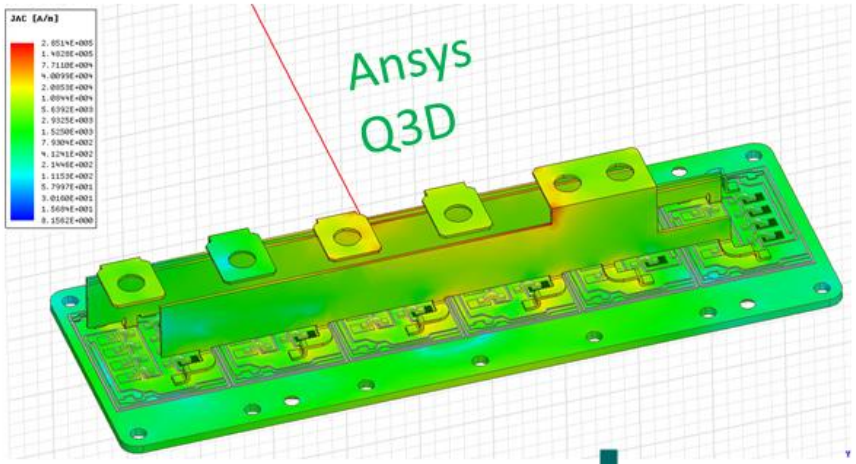
Redesign busbar structure of the module

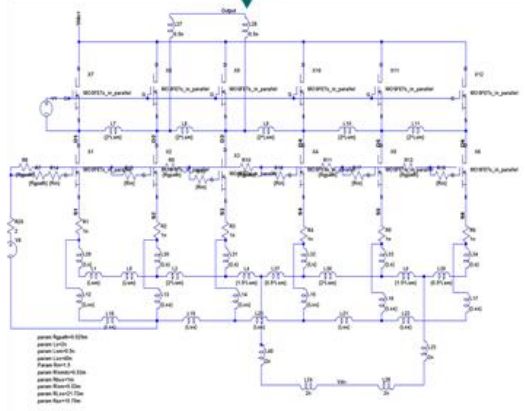
- Redirect the current flow
- Reduce Ls mismatch
- Reduce di/dt applied on mismatched Ls

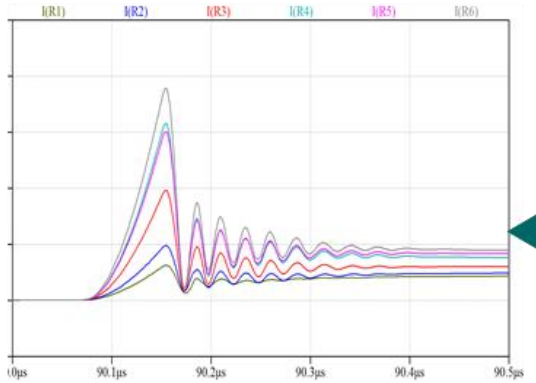


Simulation Tool









Optimized?

No

YES

New layout design

Next process

Optimization of multichip power module layout

- Current imbalance causes:
  - Mismatch of common source stray inductance
  - di/dt applied on the mismatched Ls
- Effective methods for current imbalance mitigation
  - Reduce the mismatch of common source stray inductance
  - Reduce the di/dt on the mismatched common source stray inductance
  - The key is to reduce the voltage potential differences between paralleled MOSFET source pads

Parallel Connection of SiC MOSFETs

Thanks!

helong.li@hfut.edu.cn

Part II – Active Current Sharing Methodologies

- Two types of current imbalance: Static and transient
- Active current sharing methodologies
  - Passives-based current sharing strategy
  - Driver-based current sharing strategy
- Conclusions and insight

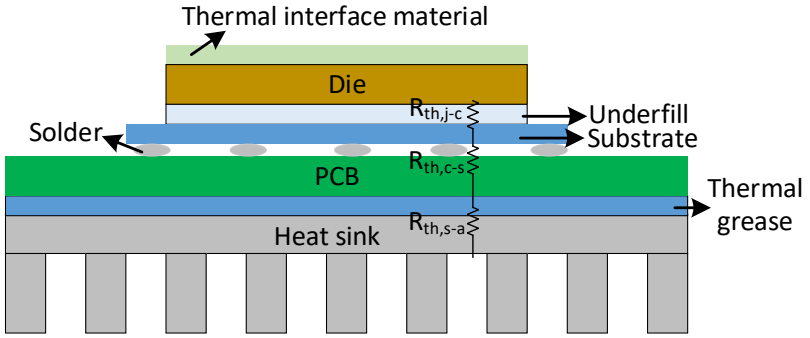
Part II – Active Current Sharing Methodologies

01

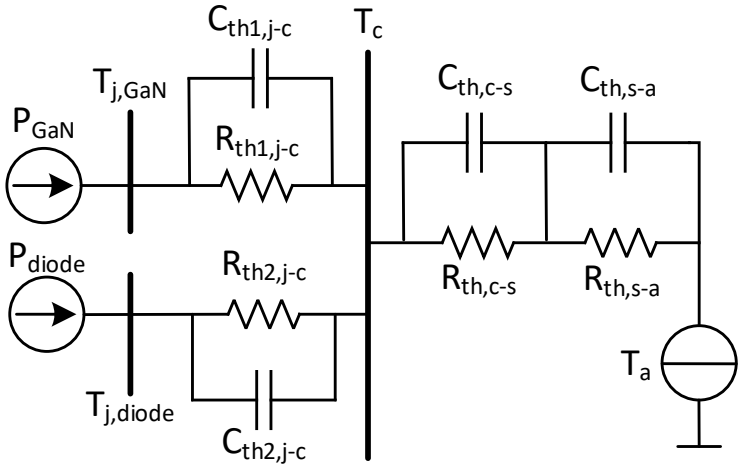
Two types of current imbalance

Two Types of Current Imbalance: Static and transient

Why does current sharing matter? – 1. Thermal issue



A typical structure of power device



The thermal network of the converter.

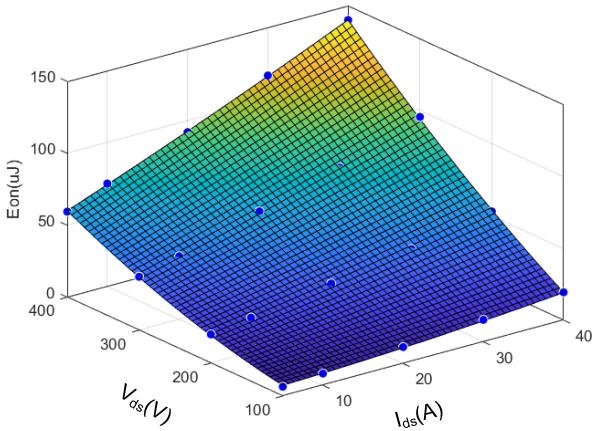
Power loss determines junction temperature!

- Two types of power loss

Conduction loss $P_{cond} = I_{rms}^2 R_{ds,on}$

Switching loss $P_{sw} = f_{sw}\, E_{sw} = \int V_{ds} I_{ds} dt$

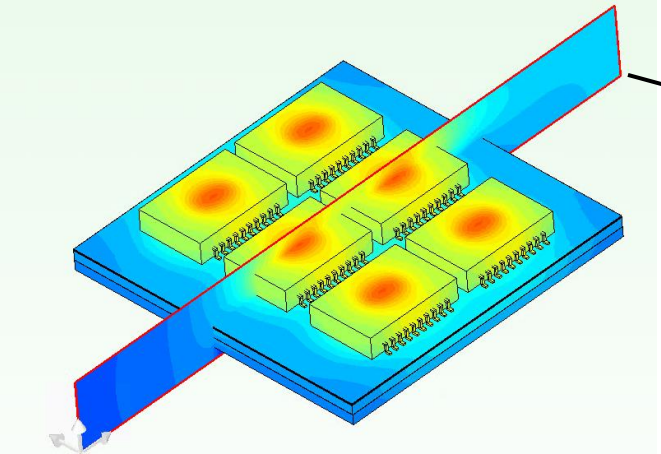
Double pulse test setup



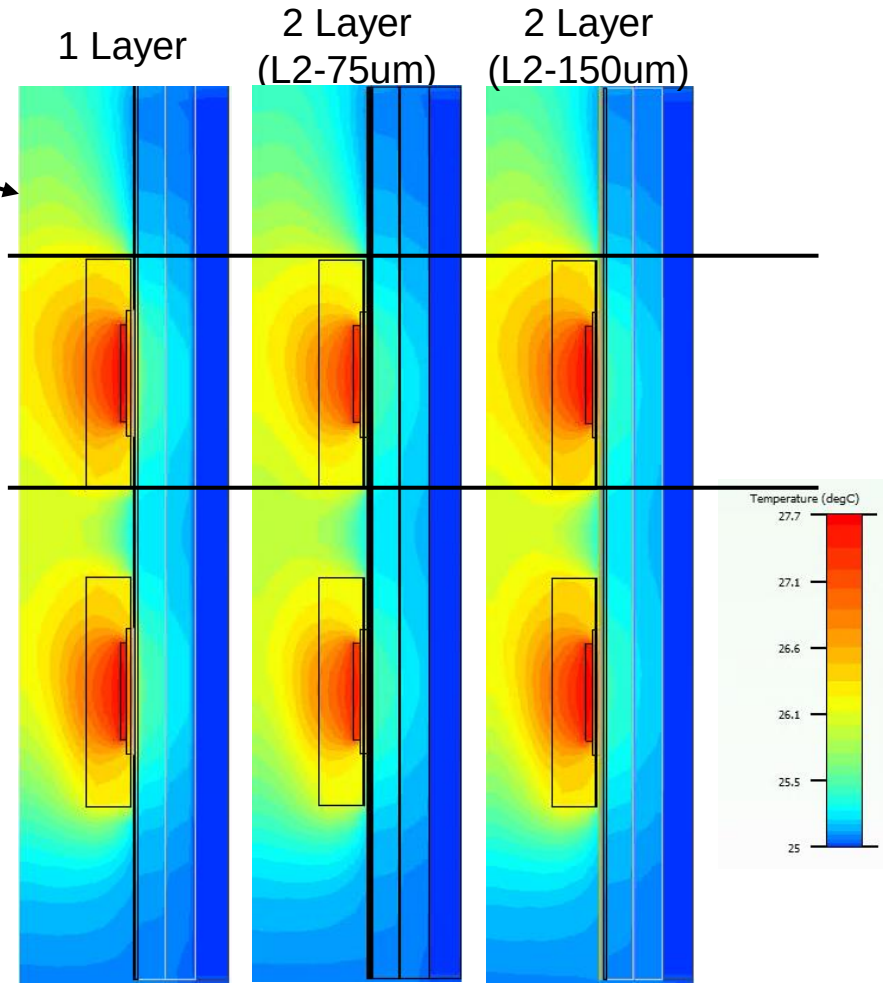
Switching loss characterization

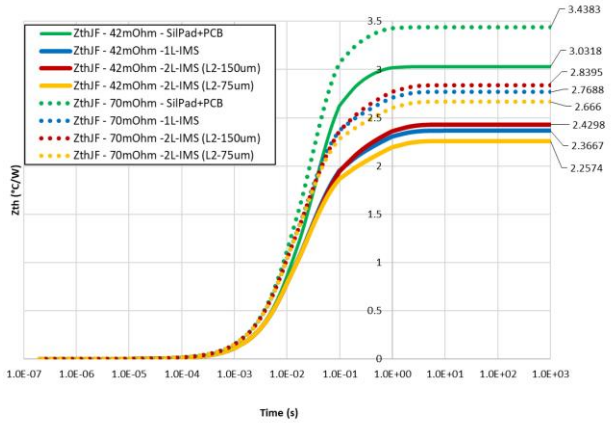
Two Types of Current Imbalance: Static and transient

Why does current sharing matter? – 1. Thermal issue



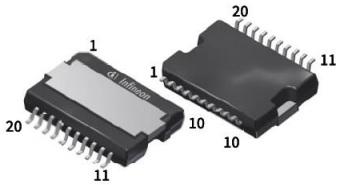
The Flotherm simulation model of the device in DSO package





$$T_j = P_{loss}\left(R_{th,j-c} + R_{th,c-s} + R_{th,s-a}\right) + T_a$$

$$Z_{th(j-c)} = \frac{R_{th(j-c)}}{1 + j \cdot 2\pi f C_{th} \cdot R_{th}}$$

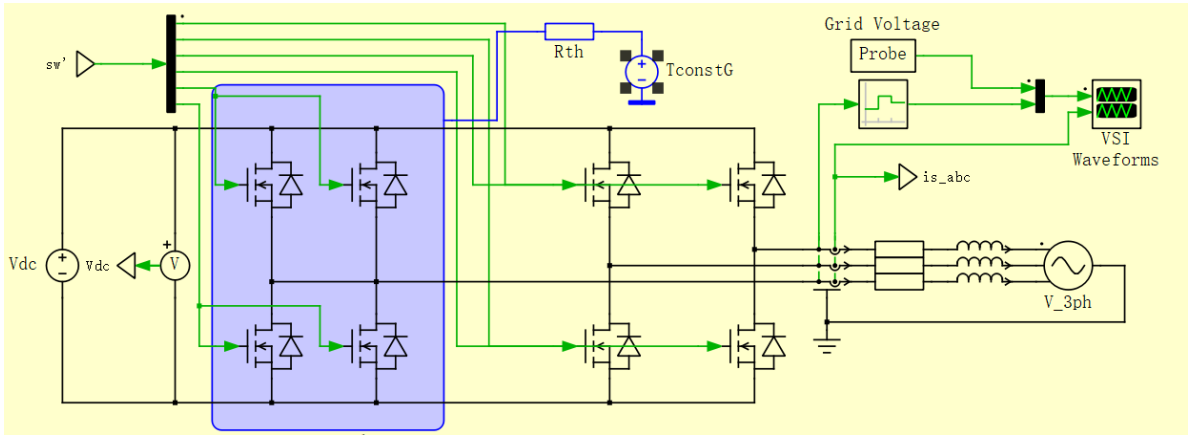


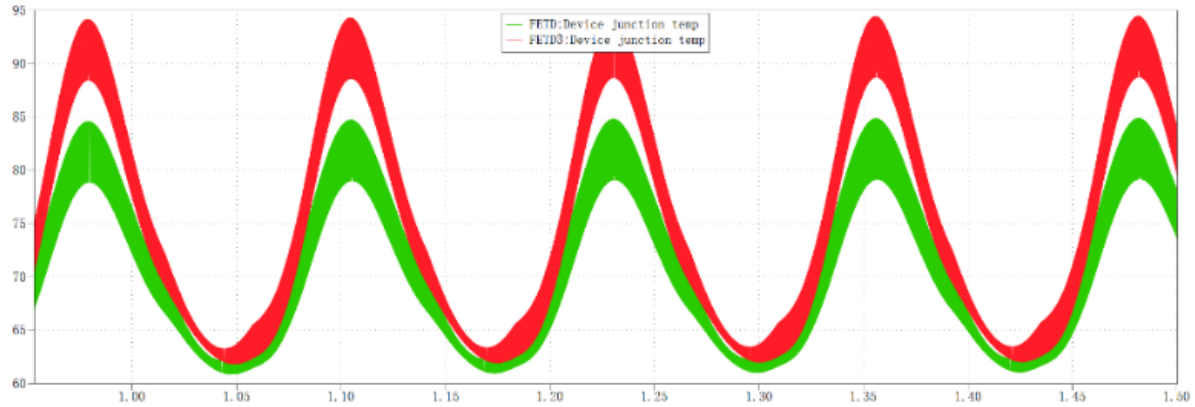
Top Side Cooled DSO

Bottom Side Cooled DSO

Two Types of Current Imbalance: Static and transient

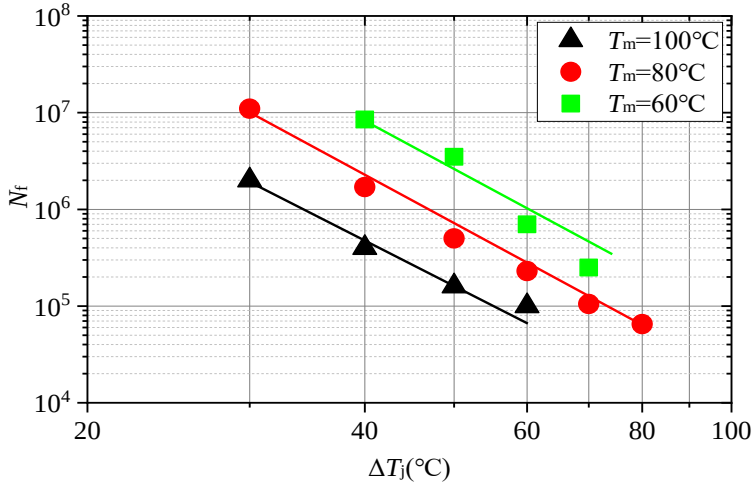
Why current sharing matters? – 2. Reliability issue (lifetime)





Coffin-Manson lifetime formula

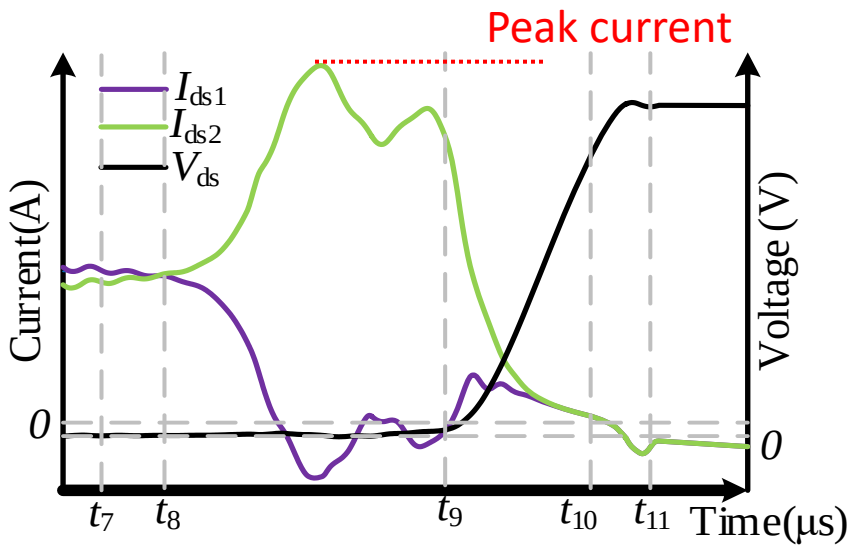
$$N_f = A \cdot \left(\Delta T_j\right)^{\alpha} \cdot e^{E_a/(k_B \cdot T_m)}$$



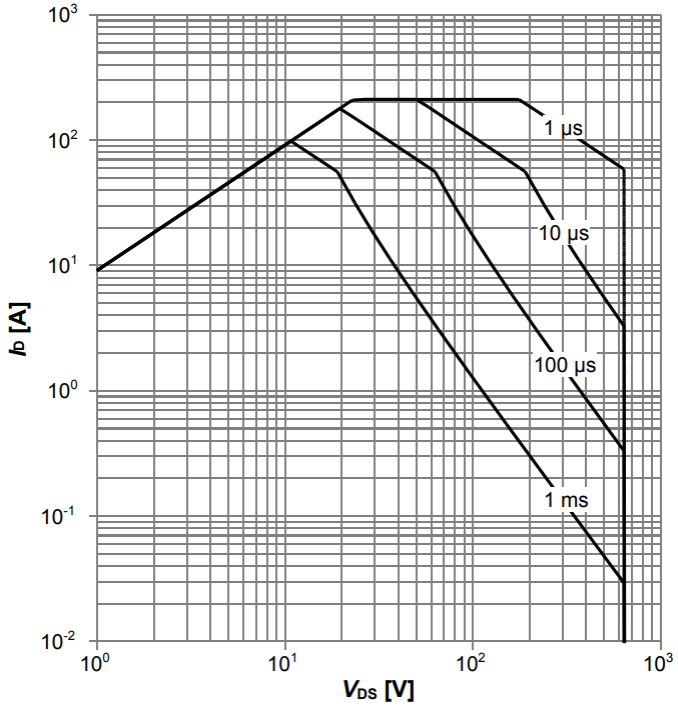
The mismatching of I_{ds} can increase the $T_{j,max}$ and raise long-term reliability concern

Two Types of Current Imbalance: Static and transient

Why does current sharing matter? – 2. Reliability issue (SOA)



The worst case of current imbalance during turn-off transient



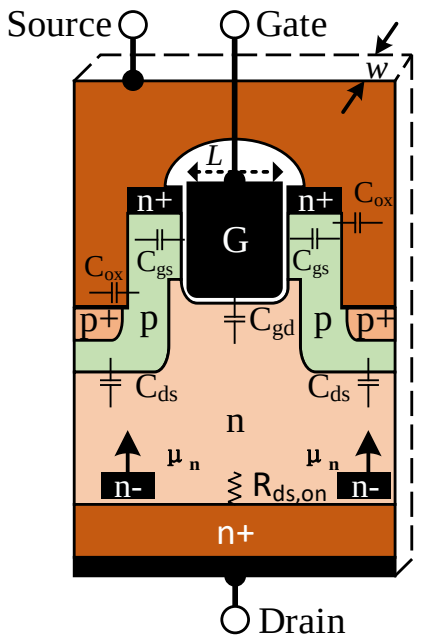
A typical safe operating area (SOA) of SiC MOSFET

- Catastrophic results:

  Very high degree of imbalance -> Higher peak current -> Out of SOA

Two Types of Current Imbalance: Static and transient

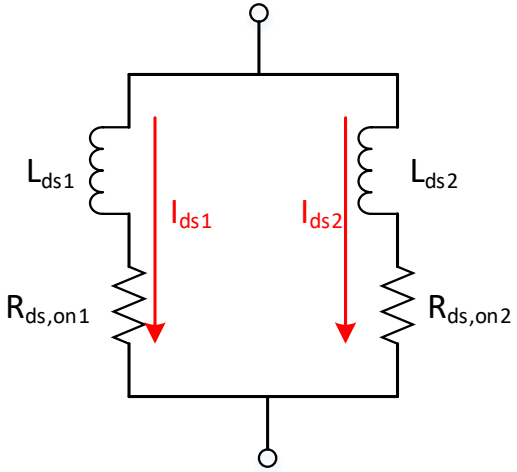
Static imbalance: higher conduction loss



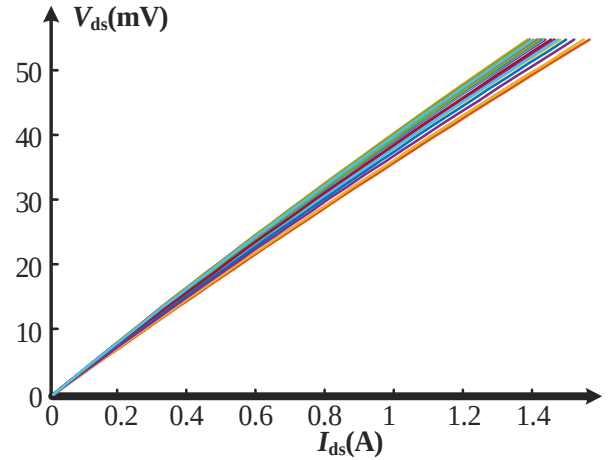
Trenchgate MOSFET

- ON-State resistance

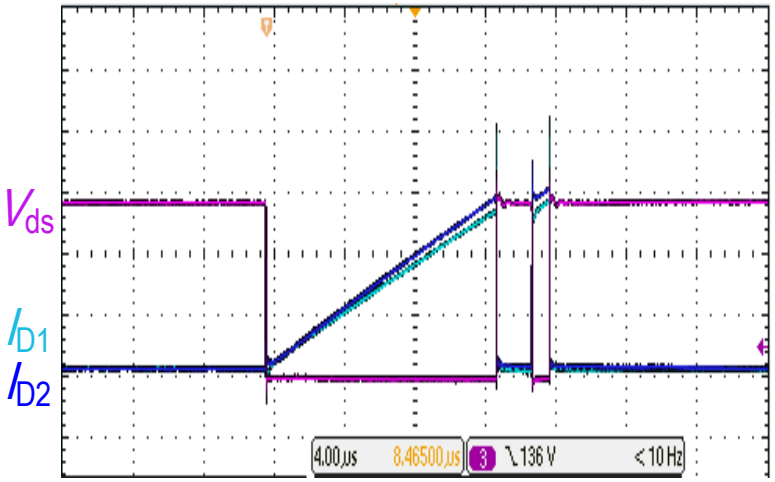
$$\begin{cases} R_{ds1\_on} = \dfrac{L}{W\mu_n C_{ox}(V_{gs1} - V_{th1})} \\ R_{ds2\_on} = \dfrac{L}{W\mu_n C_{ox}(V_{gs2} - V_{th2})} \end{cases}$$



Equivalent circuit



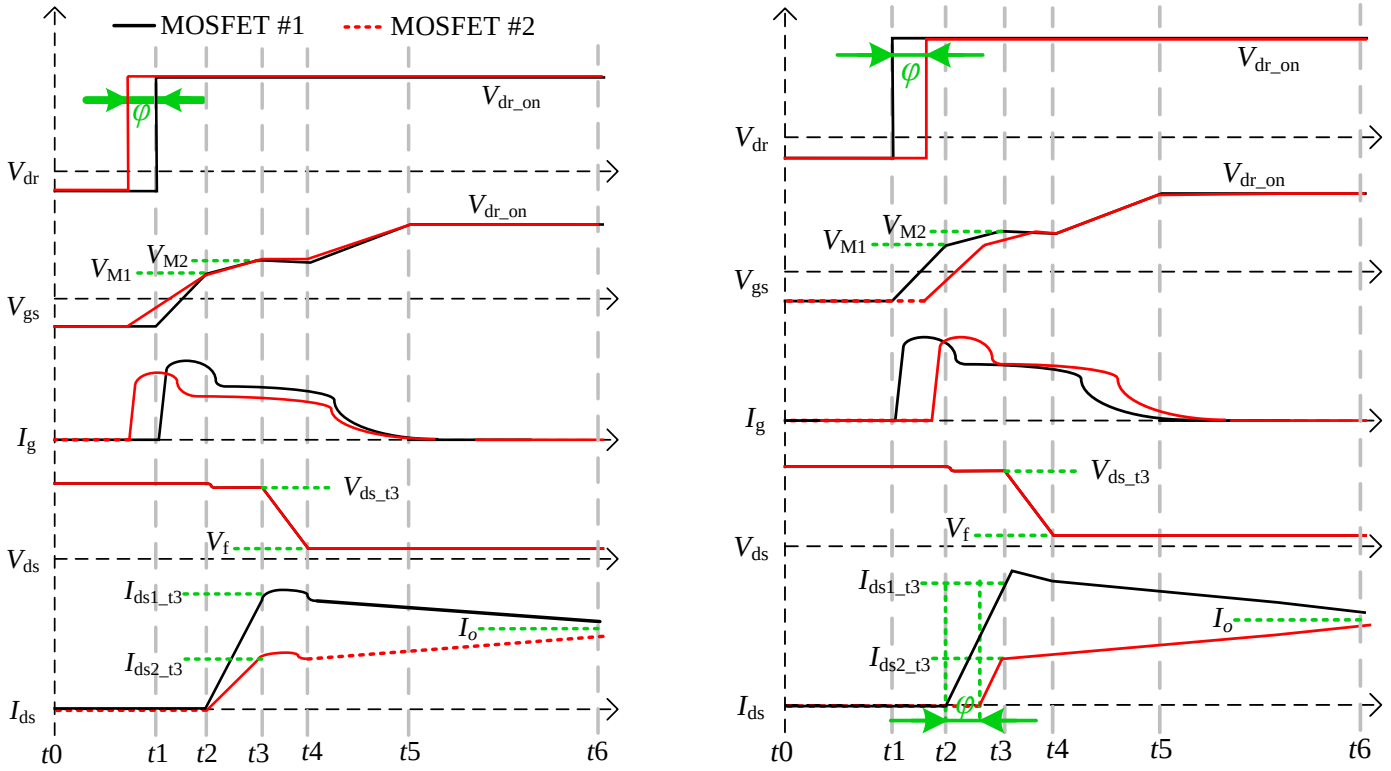
I-V curve of 20 SiC MOSFETs with same part number



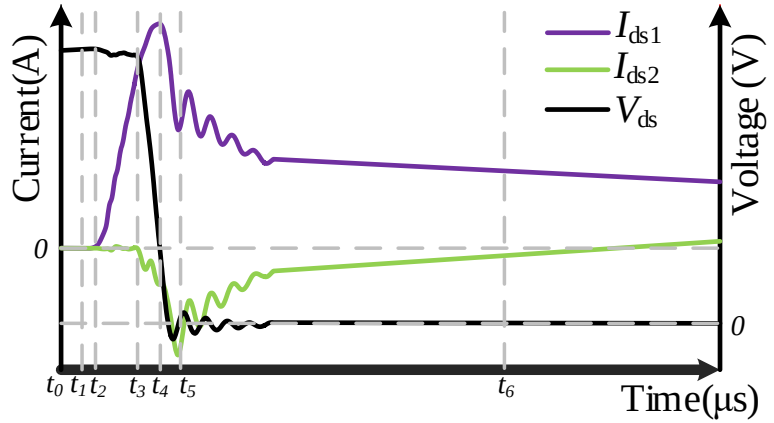
Static current imbalance

Two Types of Current Imbalance: Static and transient

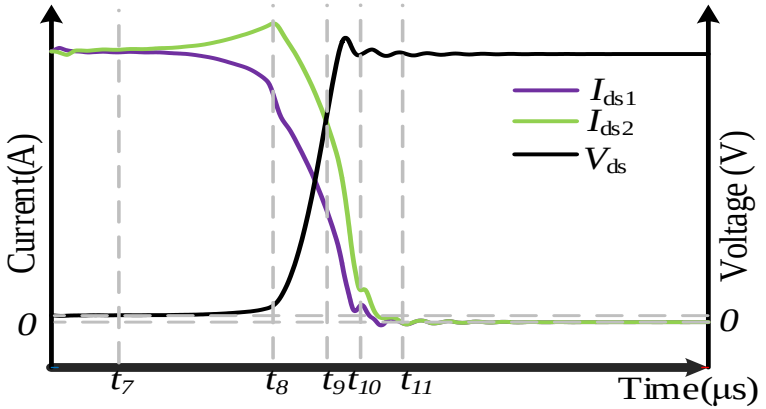
Transient imbalance: higher peak current and switching loss



Two simple modes of current imbalance:
Different switching slew rate *vs*. Asynchronous gate signal



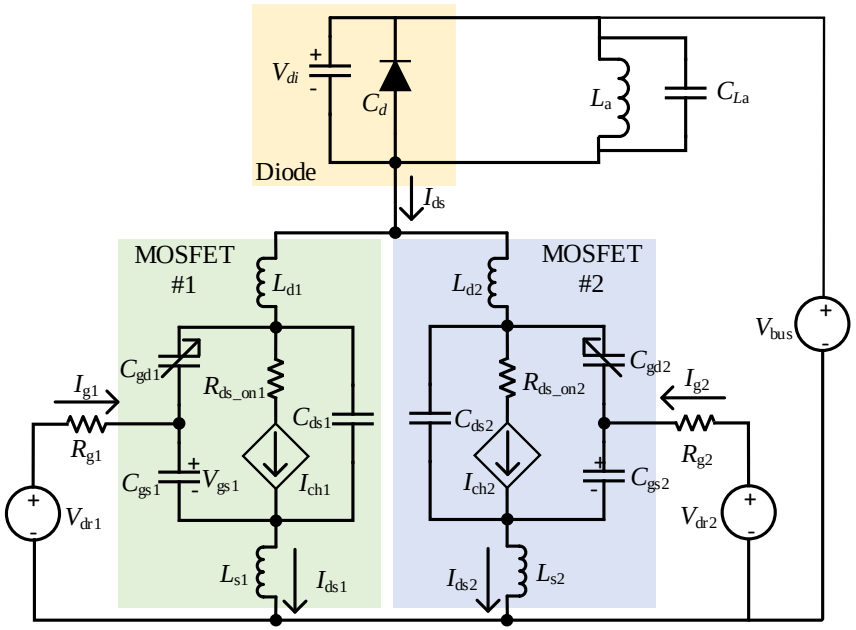
Turn-on transient imbalance



Turn-off transient imbalance

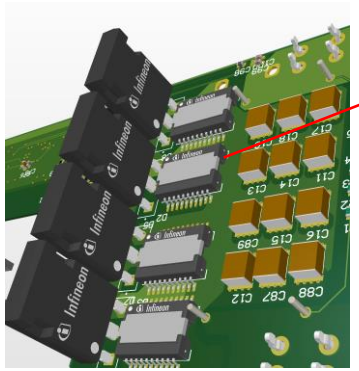
Two Types of Current Imbalance: Static and transient

What parameters impact the current distributions?



Equivalent circuit of paralleling SiC MOSFETs

Inside the package



External circuit

Some parameters that affect the current balance on parallel-connected MOSFET

Category	Variable	Definition
Intrinsic parameters	V_{th}	Gate threshold voltage
	C_{gd}	Gate-drain capacitance
	C_{gs}	Gate-source capacitance
	C_{ds}	Drain-source capacitance
	G_{fs}	Transconductance
	R_{ds_on}	On-state resistance
External parameters	V_{dr}	Driver voltage
	L_d	Drain inductance
	L_s	Source inductance
	L_g	Gate inductance
	R_g	Gate resistance
Status indicators	T_j	Junction temperature
	V_{bus}	Dc bus voltage
	I_o	Load current

02

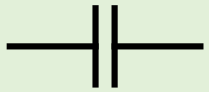
Active current sharing methodologies

Active Current Sharing Methodologies

What SOTA current sharing strategies do we have?

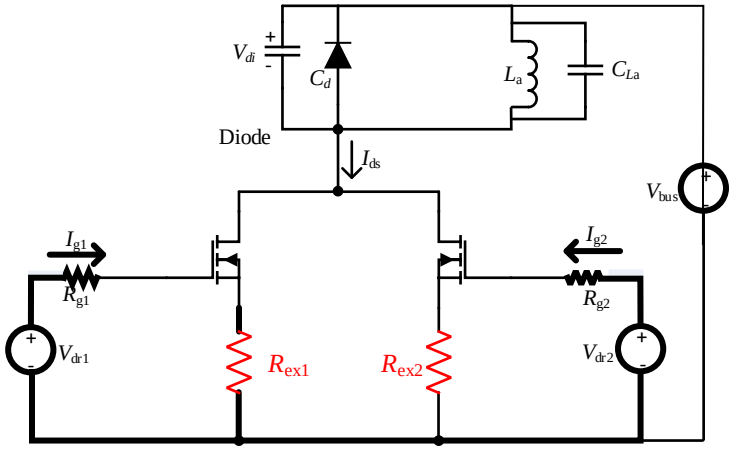
Passives-based sharing methodologies: employing external passive component to adjust the electrical parameters of the circuit

Resistor

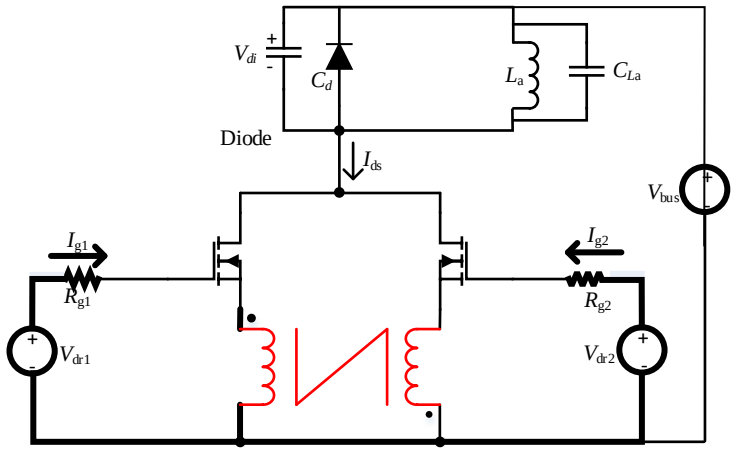


Inductor

Capacitor



External series resistor: For static imbalance

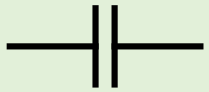


External magnetics: For transient imbalance

[1] L. Wang et al., "Cu clip-bonding method with optimized source inductance for current balancing in multichip SiC MOSFET power module," IEEE Trans. Power Electron., vol. 37, no. 7, Jul. 2022.
[2] H. Wang， F. Wang, Power MOSFETs paralleling operation for high power high density converters, in Proc. IEEE IAS Annual Meeting Industry Applications Conference. Tampa,FL,USA, 2006.
[3] Z. Zeng et al., “Imbalance current analysis and its suppression methodology for parallel SiC MOSFETs with aid of a differential mode choke,” IEEE Trans. Ind. Electron., vol. 67, no. 2, 2020.

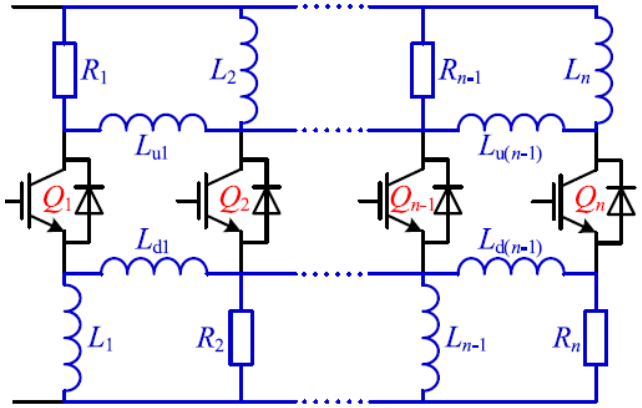
Active Current Sharing Methodologies

Resistor

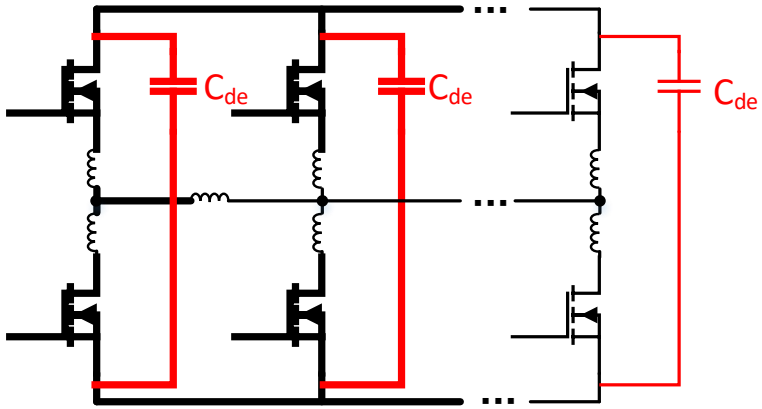


Inductor

Capacitor



Hybrid passives: RLL network

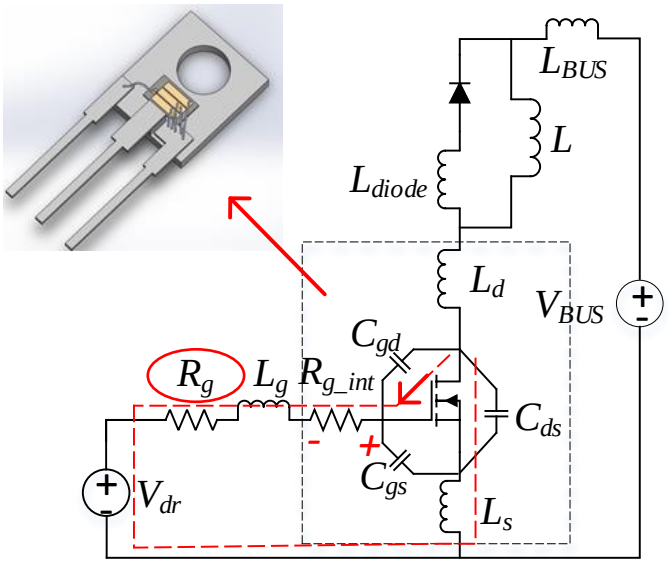


External parallel capacitors: For transient imbalance on HB

[1] J. Qu, Q. Zhang, X. Yuan and S. Cui, "Design of a paralleled SiC MOSFET half-bridge unit with distributed arrangement of DC capacitors," IEEE Trans. Power Electron., vol. 35, no. 10, pp. 10879-10891, Oct. 2020. .
[2] Y. Wang, J. Wang, F. Liu, Q. Liu and R. Zou, "An RLL current sharing snubber for multiple parallel IGBTs in high power applications," IEEE Trans. Power Electron., vol. 37, no. 7, pp. 7555-7561, Jul. 2022.

Active Current Sharing Methodologies

How can we adjust static current distribution? – Adjustable Vgs
How can we adjust the switching transient? – Maybe Rg?

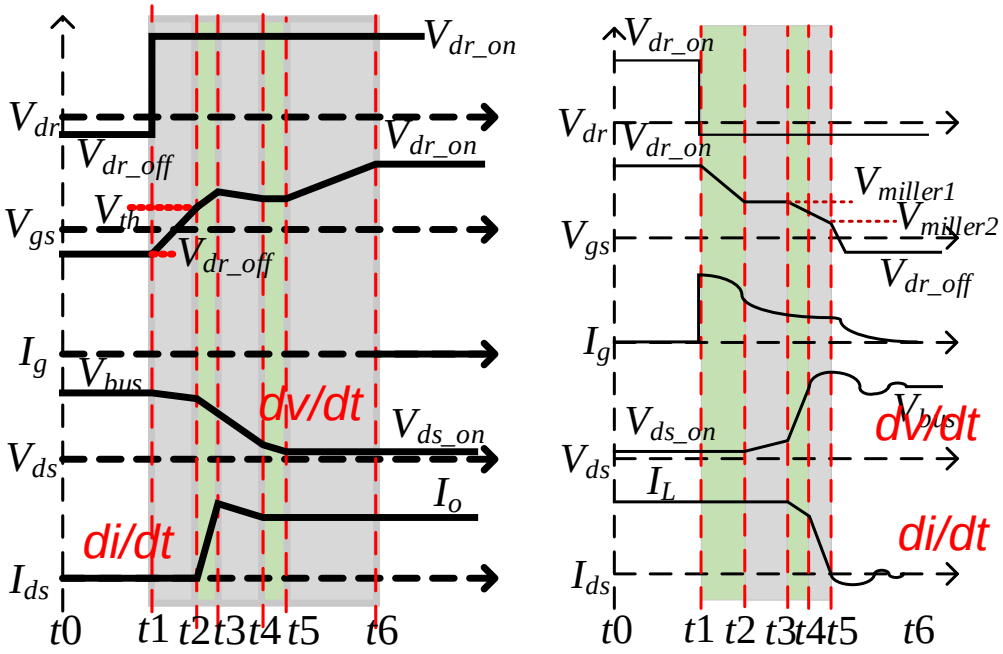


❑ The equivalent circuit of a power MOSFET

C_{gd}: Miller capacitor

C_{gs}: gate-source capacitor

L_s, L_d: parasitic stray inductance

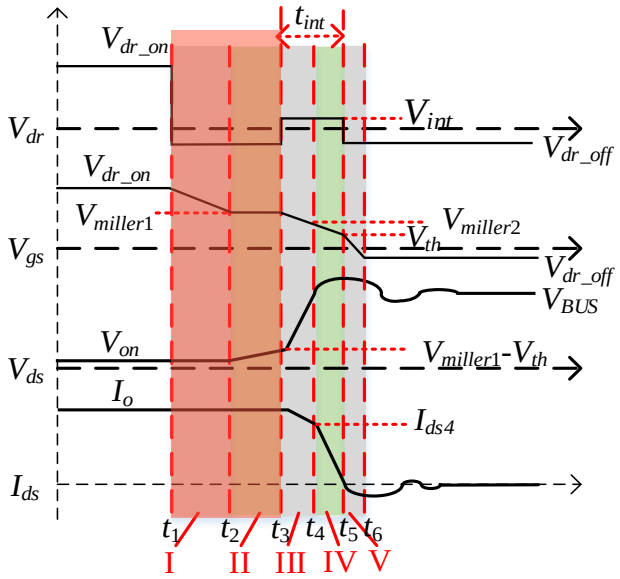


Normal turn-on Normal turn-off

- ❖ Fast switching -> Lower losses -> High EMI noise
- ❖ Switching speed cannot be adjusted actively
- ❖ Adjusting the switching speed through changing R_g

What parameters impact the switching transient? – Trajectory model tells you

❑ Trajectory Model Introduction: Turn-off Delay Stage (t_1 ~ t_3)

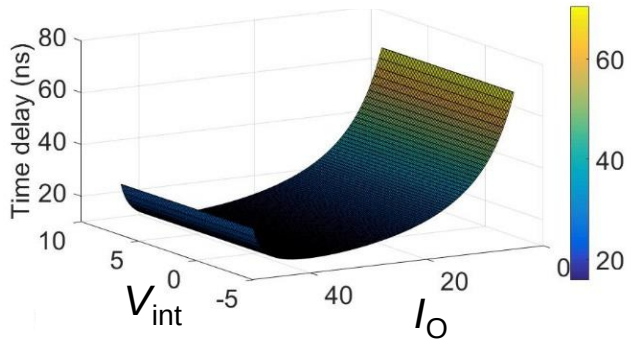


- Target: reduce the turn-off delay

Duration $t_{delay} = R_g (C_{gs} + C_{gd}) \ln(\frac{V_{dr\_on} - V_{dr\_off}}{V_{miller1} - V_{dr\_off}})$

where $V_{miller1} = \frac{I_O}{g_{fs}} + V_{th}$

$V_{miller1}$: Miller plateau voltage



Conclusion:

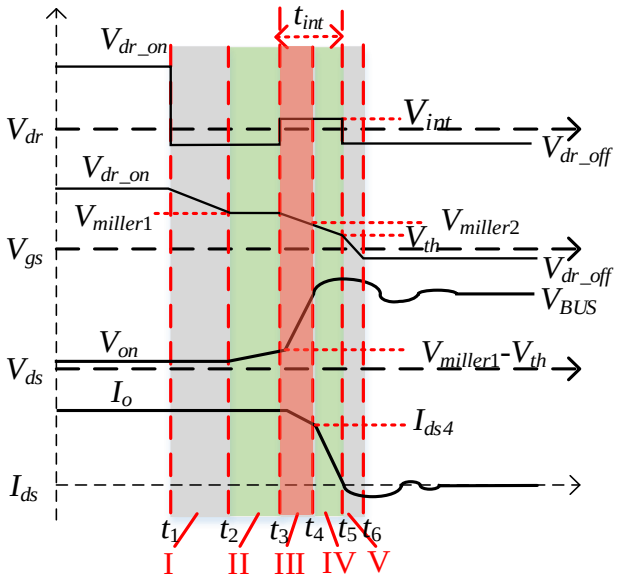
✓ Turn-off delay is related with V_{int}, but not with I_O

✓ Power losses and EMI is almost zero in this period

S. Zhao *et al*., "Adaptive multi-level active gate drivers for SiC power devices," *IEEE Transaction on Power Electronics*., vol. 35, no. 2, pp. 1882-1898, Feb 2020.

Active Current Sharing Methodologies

❑ Trajectory Model Introduction: Voltage Rising Stage (t_3 ~ t_4)

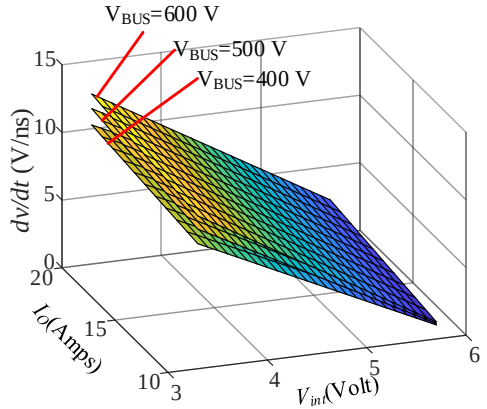


- Target: reduce the *dv/dt*
- Must consider the non-linear C_{gd}

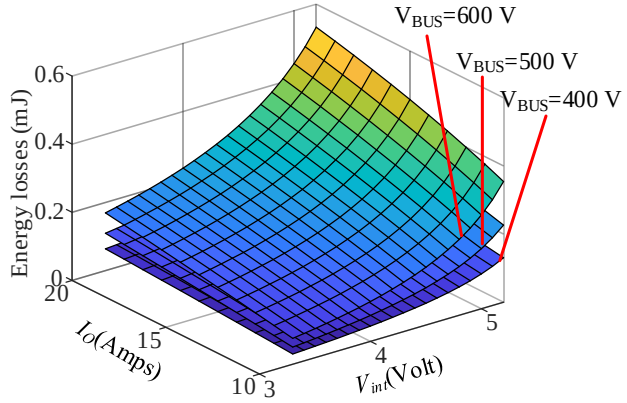
C_{gd} *vs.* V_{ds} $$C_{gd} = \frac{C_{gd0}}{\sqrt{1+V_{ds}/\phi_0}}$$

dv/dt $$\frac{dv}{dt} = \frac{V_{BUS}}{t_{VR}} = \frac{V_{BUS}\left(V_{miller1} - V_{int}\right)}{4C_{gd0}R_g\phi_0\left(\sqrt{1+V_{BUS}/\phi_0}-1\right)}$$

Energy loss $$E_{VR} = \int_{t=0}^{t_{VR}} V_{ds} I_{ds}\, dt = \frac{dv}{dt}\frac{\left(2I_{ds4}+I_O\right)t_{VR}^2}{6}$$



dv/dt vs. load current and V_{int}

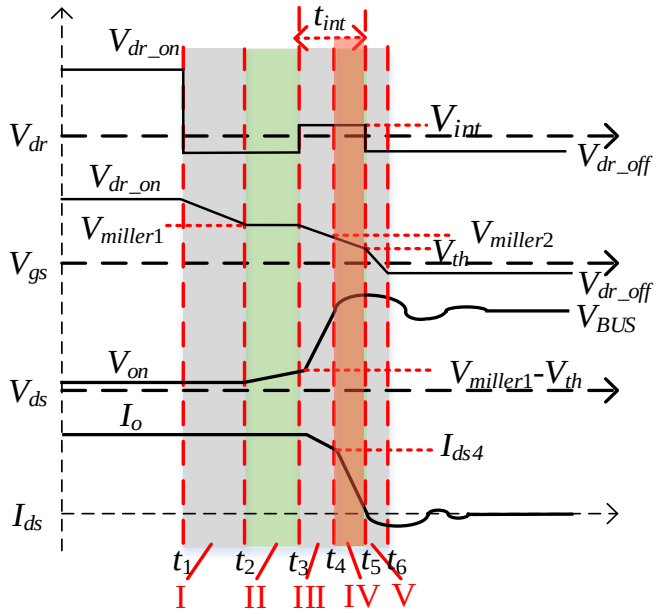


Energy losses *vs.* load current and V_{int}

- ✓ High V_{int} → Low *dv/dt* → High power losses
- ✓ The *dv/dt* and power losses are all HIGH during this period

Active Current Sharing Methodologies

❑ Trajectory Model Introduction: Current Falling Stage (t_4 ~ t_5)



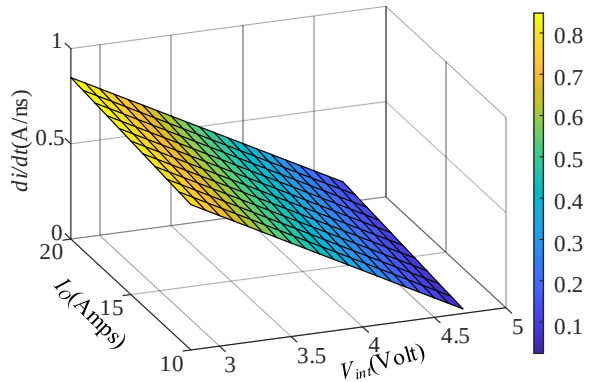
- Target: reduce the *di/dt* and voltage overshoot
- Non-saturation condition: $V_{int} < V_{th}$

di/dt

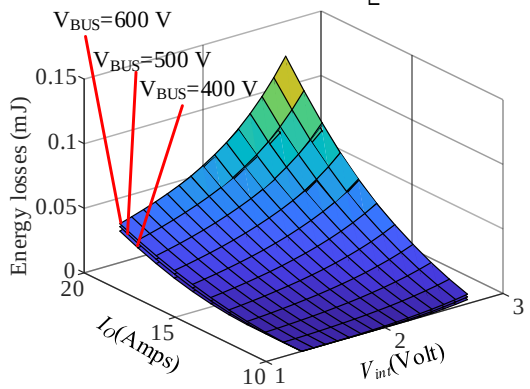
$$di/dt = \frac{I_{ds4}}{t_{CF1}} = \frac{g_{fs}\left(0.5V_{th} + 0.5V_{miller2} - V_{int}\right)}{R_g C_{iss} + L_s g_{fs}}$$

Energy loss:

$$E_{CF} = \frac{t_{CF1} V_{BUS} I_{ds4}}{2} = \left[I_O - \left(C_d + C_L\right) \frac{I_O + \left(V_{th} - V_{int}\right) g_{fs}}{2 R_g C_{gd} g_{fs}} \right] \frac{\left(R_g I_{ds4} C_{iss} + L_s g_{fs} I_{ds4}\right) V_{BUS}}{g_{fs}\left(V_{th} - V_{int}\right)}$$



The *di/dt vs.* load current and V_{int}

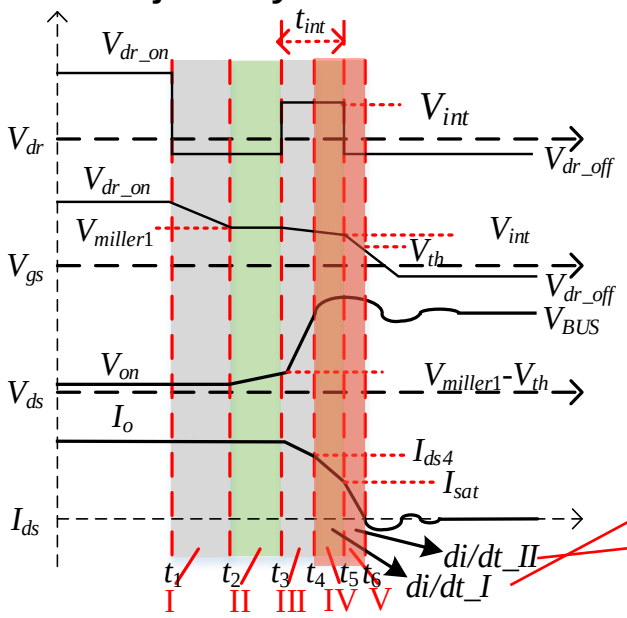


The energy losses E_{CF} *vs.* load current and V_{int}

- ✓ High V_{int} → Low *di/dt* → High power losses
- ✓ The *di/dt* and power losses are all HIGH during this period

Active Current Sharing Methodologies

❑ Trajectory Model Introduction: Current Falling Stage (t_4 ~ t_6)

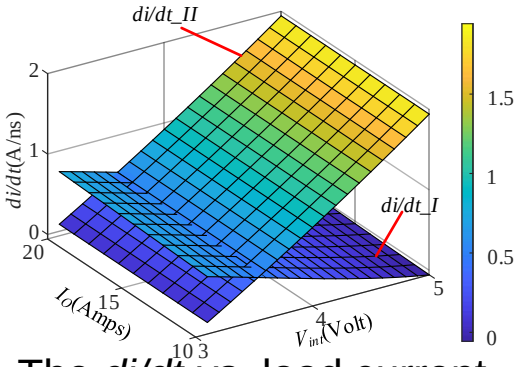


- Target: reduce the *di/dt* and voltage overshoot
- Saturation condition: $V_{int} > V_{th}$, the V_{int} is not able to completely shut down the device

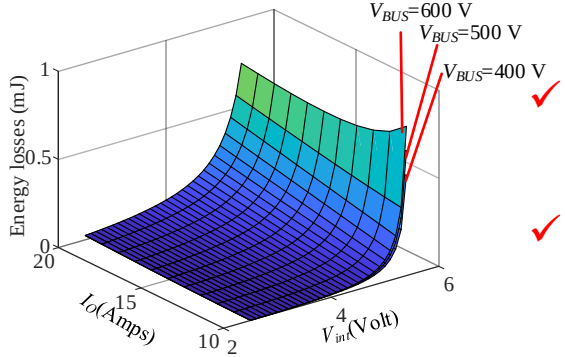
Saturation current $I_{sat} = \frac{k_p}{2}(V_{int} - V_{th})^2$

$$di/dt\_I = \frac{I_O - (C_d + C_L)(V_{BUS} - V_{miller1} + V_d + V_{th})/t_{VR} - I_{sat}}{t_{CF2}}$$

$$di/dt\_II = \frac{I_{sat}}{t_V} = \frac{I_{sat}}{(C_{gd} + C_{gs})R_g \ln\left(\frac{V_{int} - V_{dr\_off}}{V_{th} - V_{dr\_off}}\right)}$$



The *di/dt vs.* load current and V_{int}



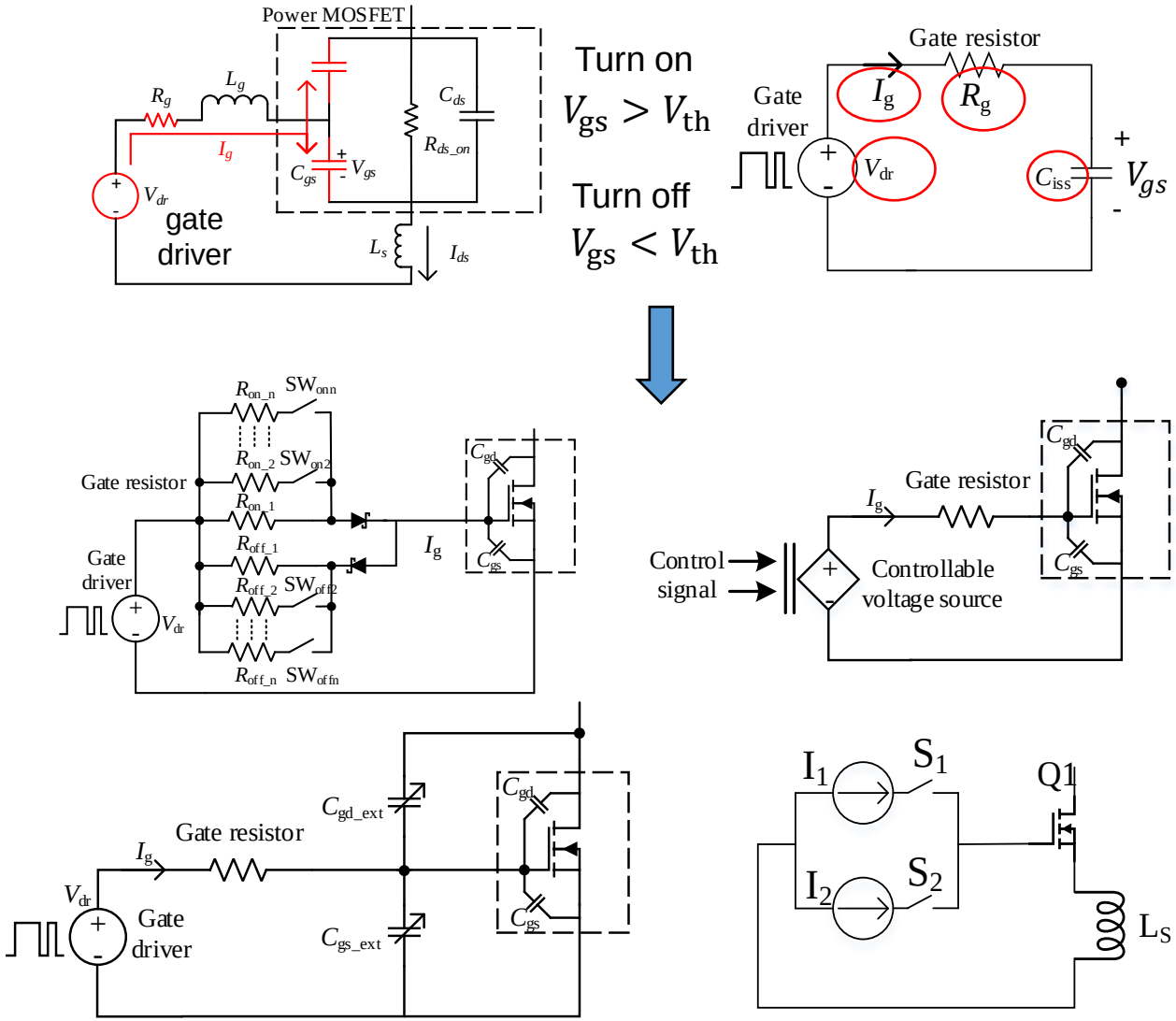
The energy losses E_{CF} *vs.* load current and V_{int}

- ✓ High V_{int} → Low *di/dt_I* → High *di/dt_II* → High power losses
- ✓ The *di/dt* and power losses are all HIGH during this period

Active Current Sharing Methodologies

Conclusions: How can we implement switching process control?

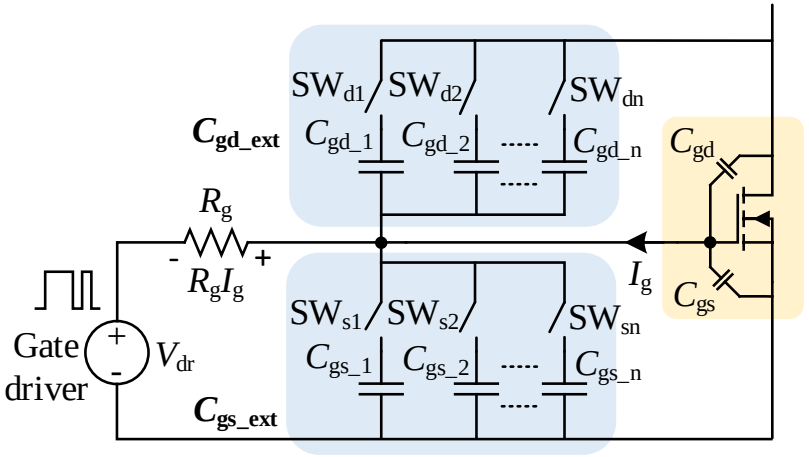
- Five freedoms: R_g, C_{iss}, I_g, V_{dr}, and time delay
- Five State-of-the-Art AGD Methodologies
  - Change R_g: Variable gate resistance method
    - Easy to implement, low resolution
  - Change C_{iss}: Variable input capacitance method
    - Hard to change capacitance actively
  - Change I_g: Variable gate current method
    - Good oscillation suppression, remove R_g
    - Hard to design
  - Change V_{dr}: Variable gate voltage method
    - Easy to implement DESAT protection
    - High resolution, easy adjustment
  - Change *delay*: Variable delay time method
    - Easy to implement DESAT protection
    - High resolution, easy adjustment



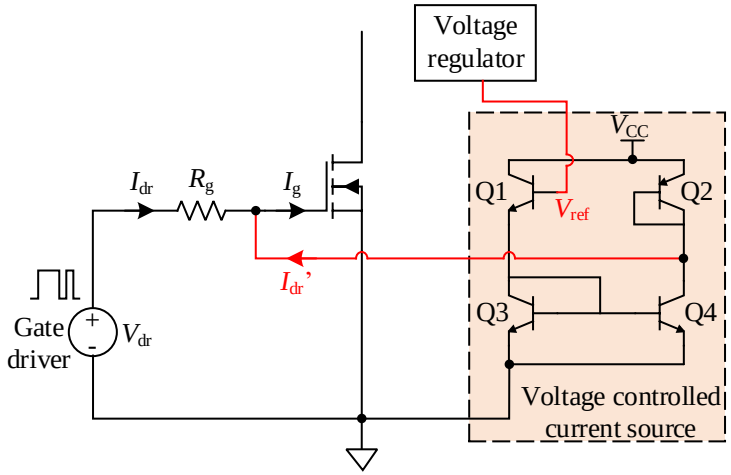
S. Zhao, X. Zhao, Y. Wei, Y. Zhao and H. A. Mantooth, "A review on switching slew rate control for silicon carbide devices using active gate drivers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4096-4114, Jul. 2020.

Active Current Sharing Methodologies

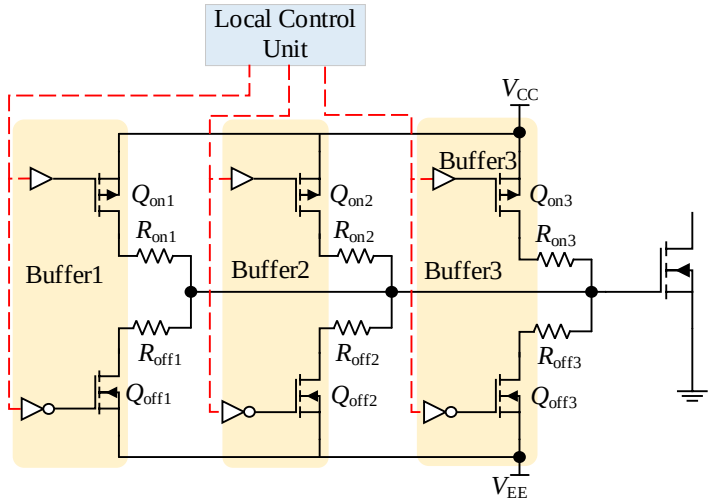
What SOTA AGD circuitries do we have now?



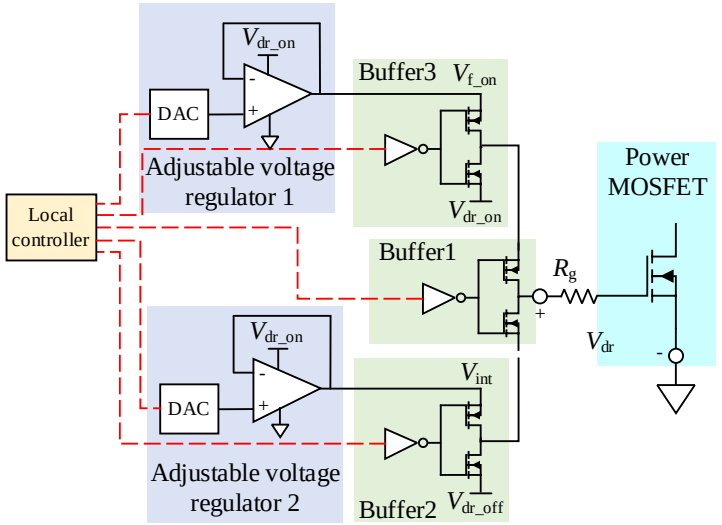
Variable gate capacitance



Variable gate current (Sun, VT, 2019)



Variable gate resistance (Engelmann, RWTH Aachen, 2019)



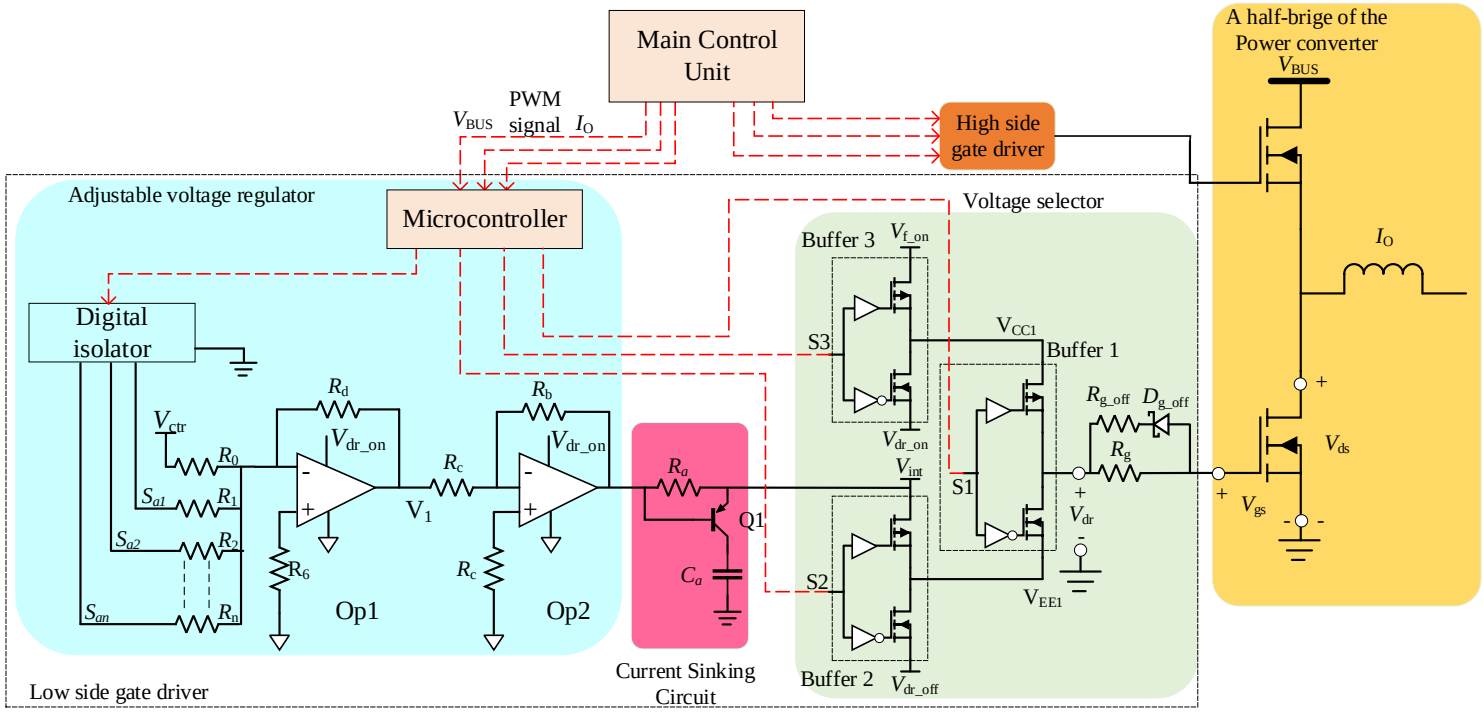
Variable gate voltage (Zhao, UArk, 2020)

[1] G. Engelmann, T. Senoner and R. W. DeDoncker, "Experimental investigation on the transient switching behavior of SiC MOSFETs using a stage-wise gate driver," *CPSS Trans. Power Electron. Appl.*, vol. 3, no. 1, pp. 77-88, 2018.

[2] Sun, R. Burgos, X. Zhang and D. Boroyevich, "Active dv/dt control of 600V GaN transistors," in Proc. Energy Conv. Congr. Expo., Milwaukee, WI, USA, 2016.

Active Current Sharing Methodologies

How can we implement a true AGD? – An example

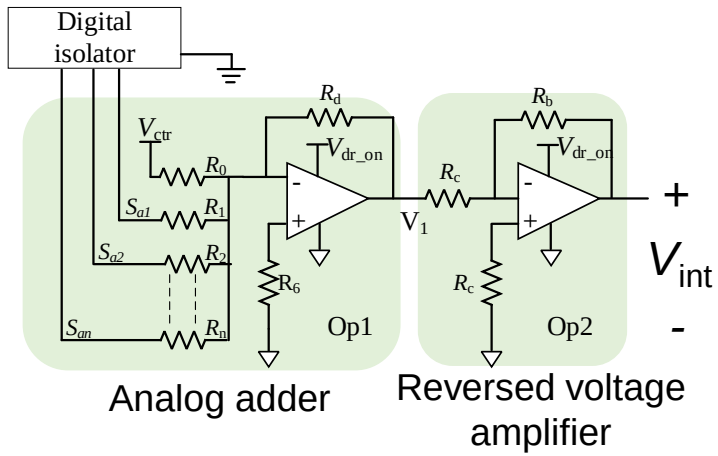


- Microcontroller: Control the AGD and conduct optimization
- Adjustable voltage regulator: generate the intermediate voltage level
- Current sinking circuit: Assist in sinking reversed flowing gate current
- Voltage selector: generate the multi-level driver voltage profile

S. Zhao, X. Zhao, A. Dearien, Y. Wu, Y. Zhao, and H. A. Mantooth, "An intelligent versatile active gate driver for high-voltage SiC MOSFET and its optimization," IEEE J. Emer. Sel. Topics Power Electron, vol.8, no.1, pp. 429-441, 2020

Active Current Sharing Methodologies

- The active voltage regulator



Output of voltage regulator

$$V_{\text{int}} = V_{\text{ctr}}\left(\frac{1}{R_0} + \frac{S_{a1}}{R_1} + \frac{S_{a2}}{R_2} \cdots \frac{S_{an}}{R_n}\right) R_{\text{d}} \frac{R_{\text{b}}}{R_{\text{c}}}$$

Herein, S_{a1}- S_{an} = 0 or 1

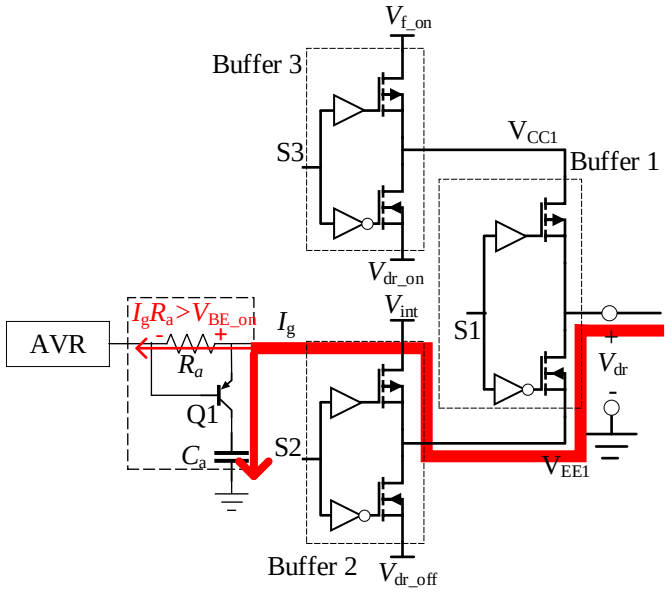
Relationship of the resistors

$$R_1 = 2^1 R_2 = 2^2 R_3 = 2^{n-1} R_n$$

- The current sinking circuit

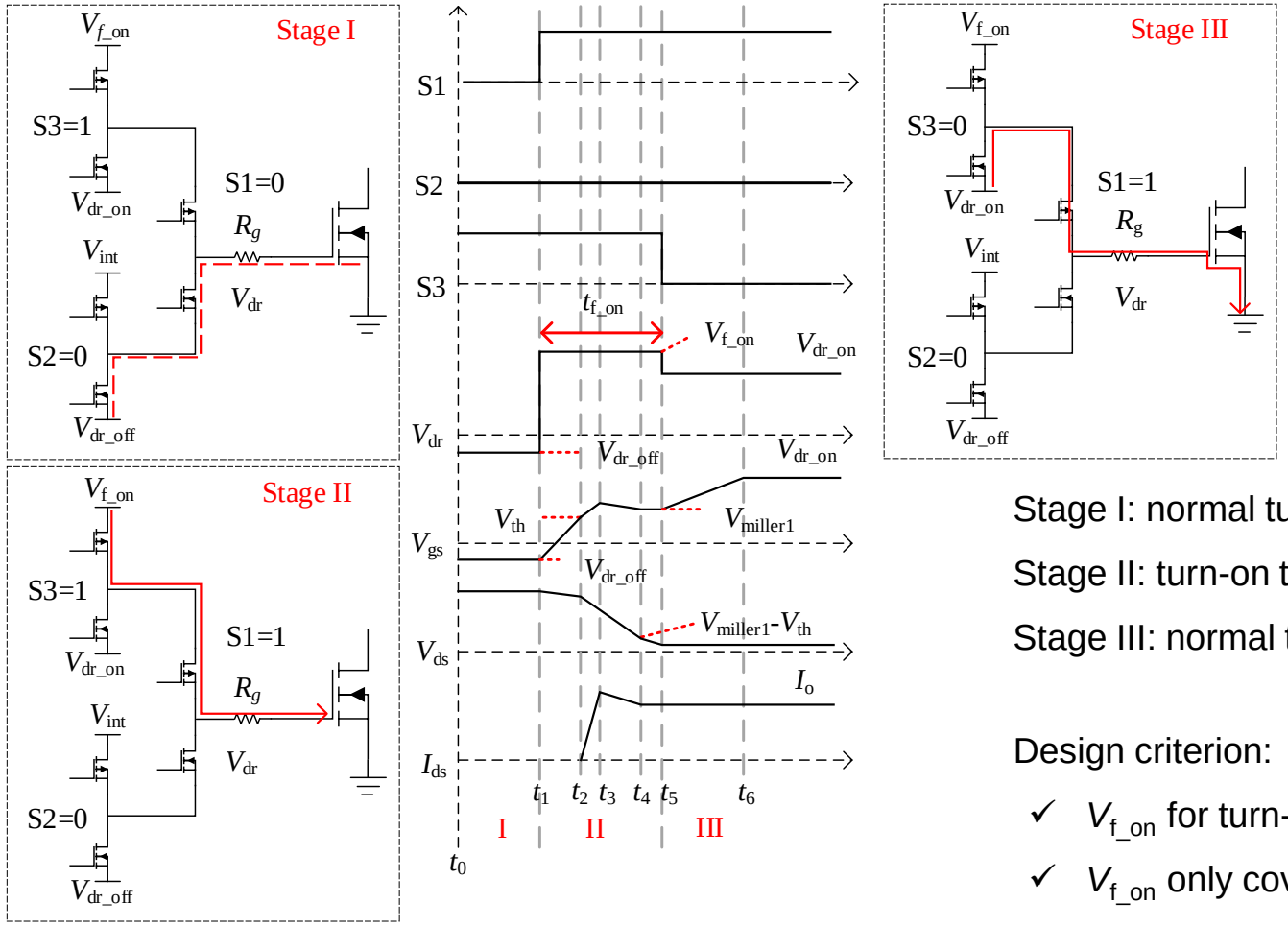
The design criterion:

$$I_{\text{g}} R_{\text{a}} \geq V_{\text{BE\_on}}$$



Active Current Sharing Methodologies

- The working principle of voltage selector: Faster turn-on



Stage I: normal turn-off

Stage II: turn-on transient

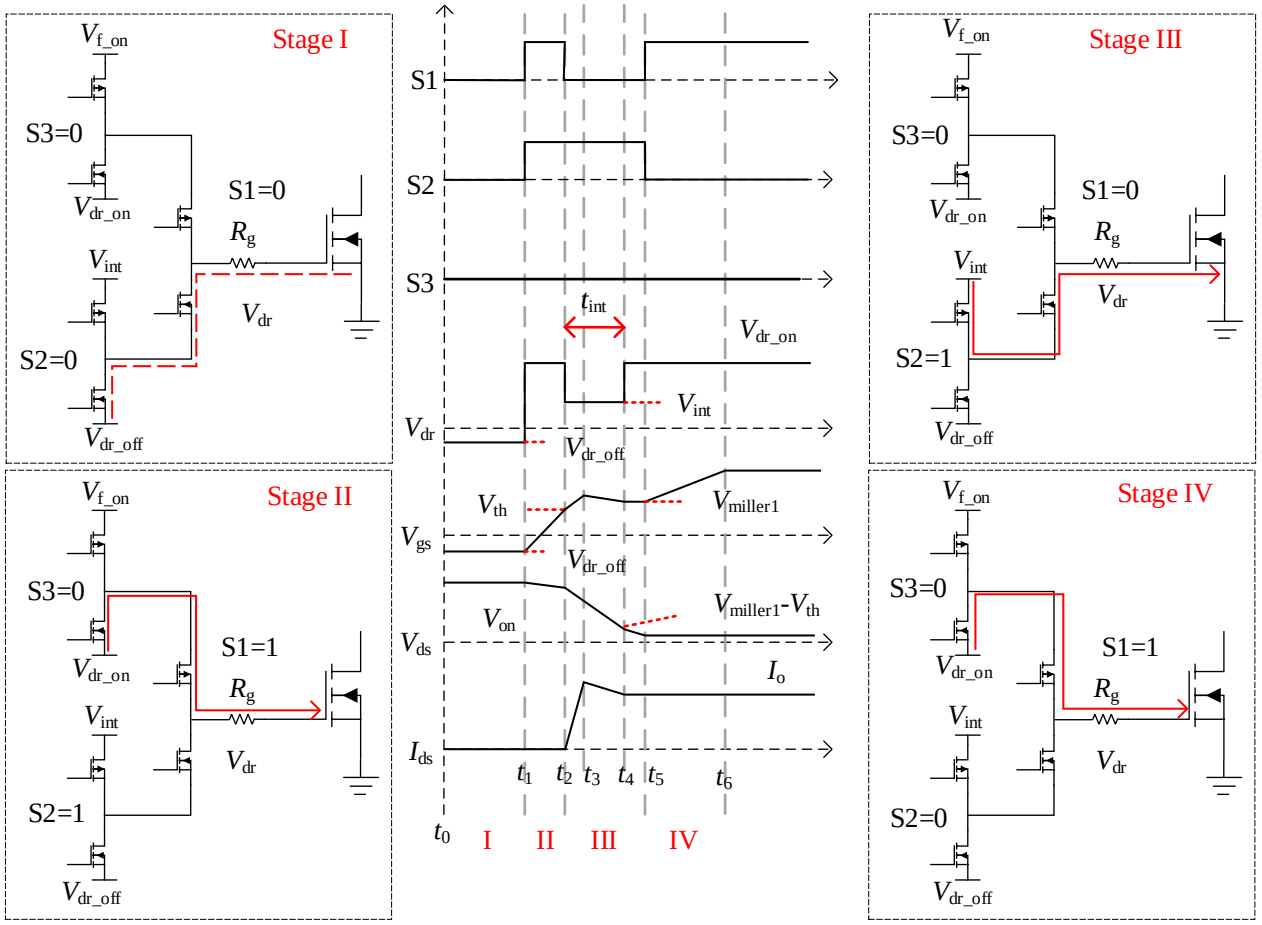
Stage III: normal turn-on

Design criterion:

- ✓ V_{f_on} for turn-on transient
- ✓ V_{f_on} only covers t_1 - t_5

Active Current Sharing Methodologies

- The working principle of voltage selector: Slower turn-on



Stage I: normal turn-off

Stage II: turn-on delay

Stage III: Miller plateau

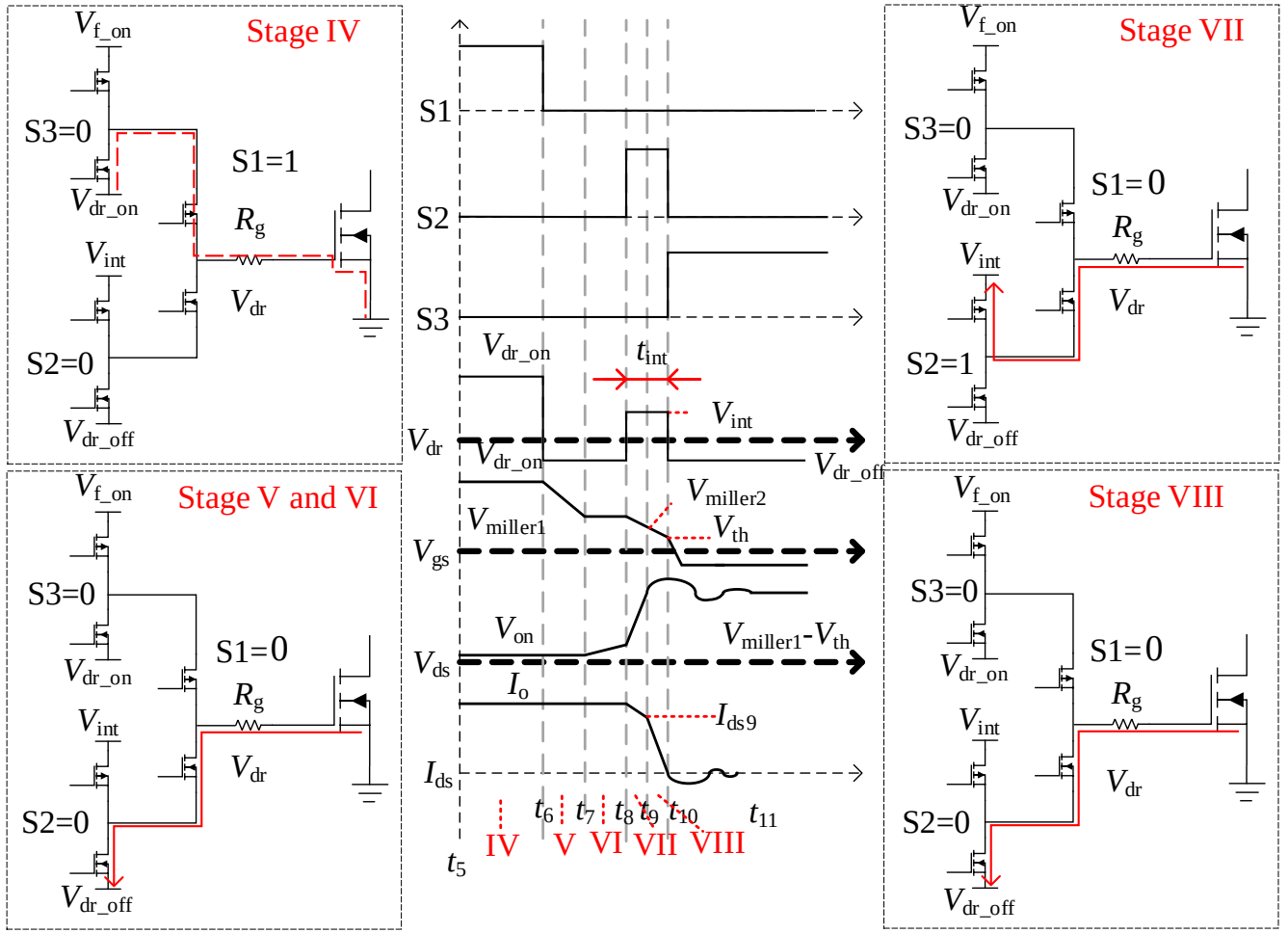
Stage IV: normal turn-on

Design criterion:

- ✓ V_{dr_on} for shortening turn-on delay
- ✓ V_{int} only covers voltage falling time and current rising time
- ✓ V_{dr_on} for normal turn-on condition

Active Current Sharing Methodologies

- The working principle of voltage selector: Slower turn-off



Stage IV: normal turn-on

Stage V: turn-off delay

Stage VII: Miller plateau

Stage VIII: normal turn-off

Design criterion:

- ✓ V_{dr_off} for shortening turn-off delay
- ✓ V_{int} only covers voltage rising time and current falling time
- ✓ V_{dr_off} for normal turn-off condition

Active Current Sharing Methodologies

How can we capture the true switching waveform of WBG? – Measurement matters!

- ❑ Measurement for SiC power MOSFET
  - ✓ Shorten the measurement loop: reduce measurement EMI

V_{ds} measure: Use BNC adaptor

V_{gs} measure: Use MMCX connector OR optical isolated probe (very expensive)

Use wire wound connection instead of alligator clip

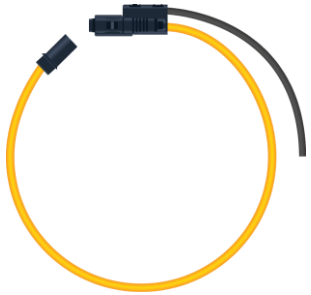
- ✓ Current measurement

T&M coaxial shunt

Paralleling SMD resistor shunt + MMCX

Shunt resistor:

- ✓ High bandwidth: >= 400 MHz
- ❖ Carefully design the grounding

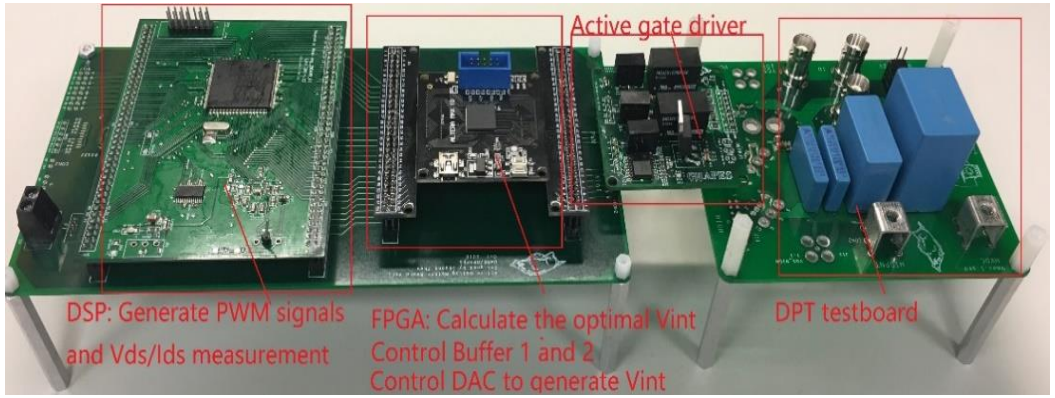


Rogowski coil

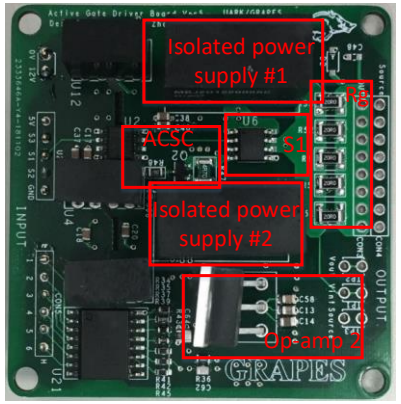
- ✓ Isolation
- ❖ Lower bandwidth: 30 MHz

Active Current Sharing Methodologies

- Designed gate driver – For 1.2 kV SiC power MOSFET



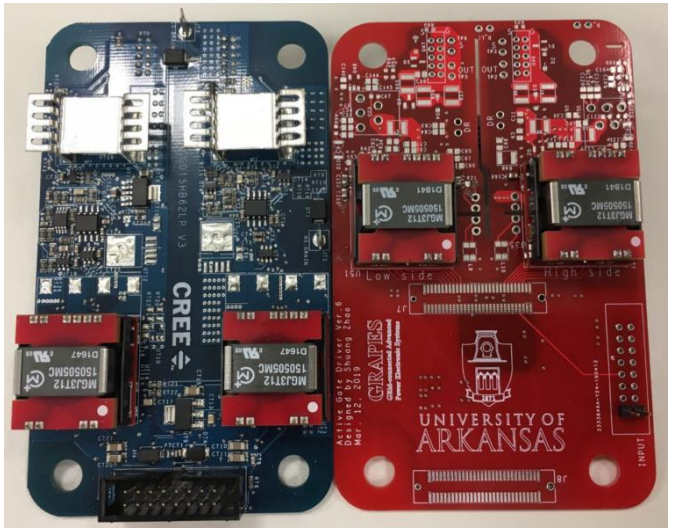
1.2 kV intelligent active gate driver setup



Active gate driver board Ver. 5

Active gate driver
- ✓ 64 levels of V_{int} adjustment
- ✓ Very fast speed: 3.3 ns
- ✓ 2.5 kV isolation levels

CREE conventional gate driver

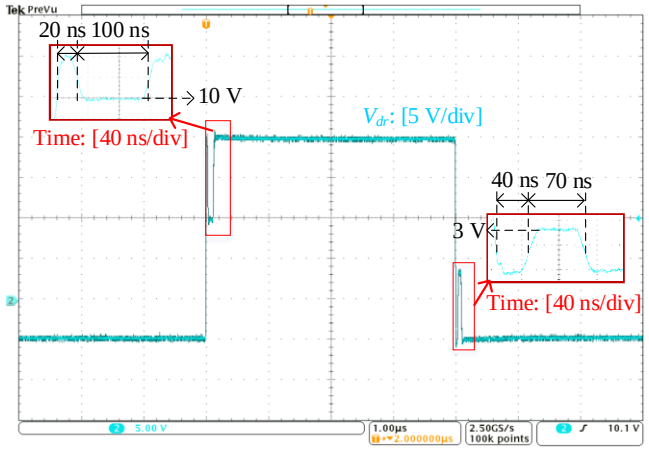


Active gate driver for 1.2 kV/300A half-bridge SiC

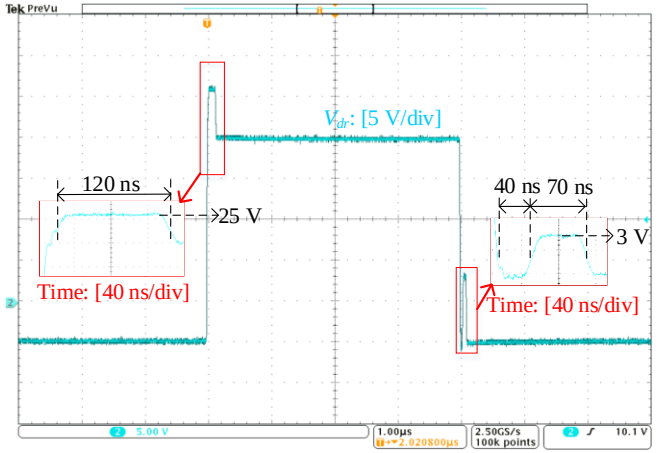
Active gate driver
- ✓ Compatible with CREE gate driver
- ✓ DESAT Protection
- ✓ Junction temperature

Active Current Sharing Methodologies

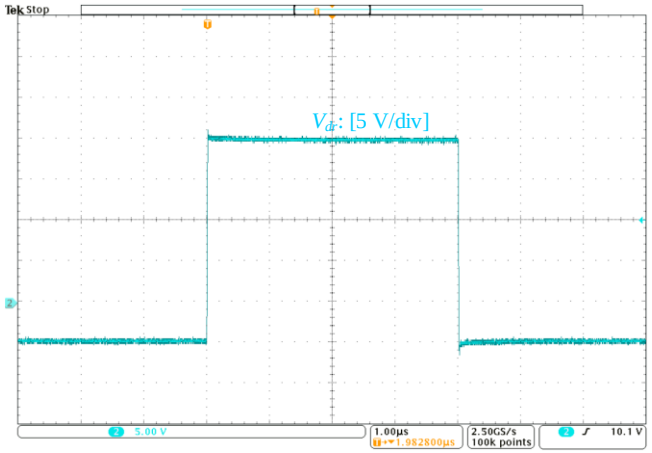
- Empty load experiments results of the AGD



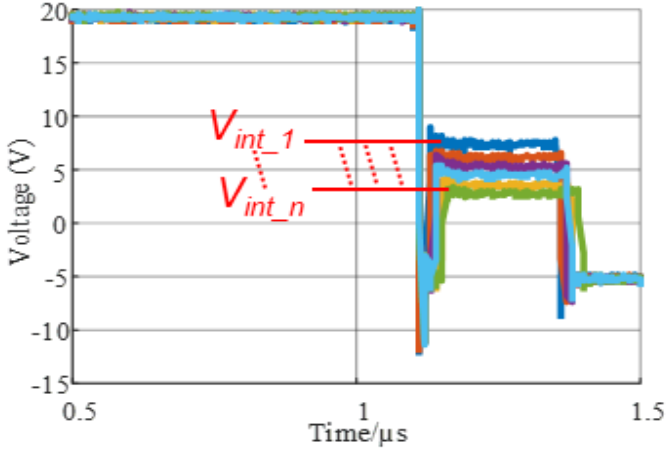
Slower turn-on and slower turn-off



Faster turn-on and slower turn-off



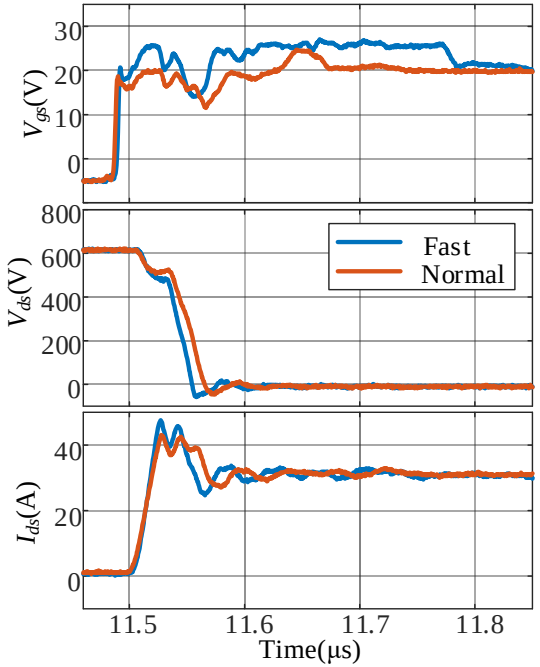
Normal turn-on and normal turn-off



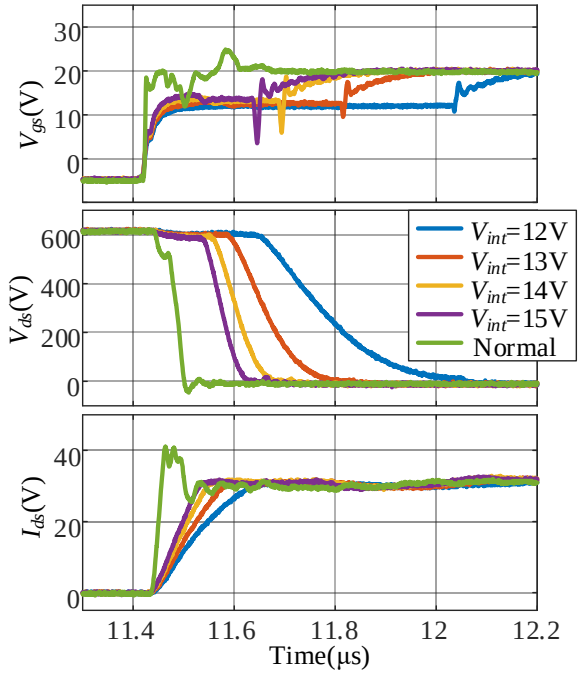
V_{int} and duration are adjustable

Active Current Sharing Methodologies

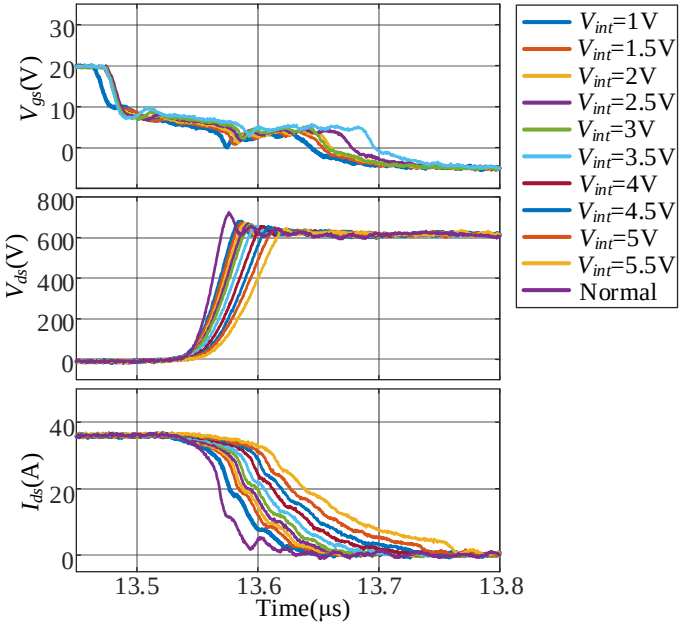
- Experimental verification on 1.2 kV devices



- Faster turn-on mode
  - ✓ Reduce turn-on losses (770 μJ -> 660 μJ, 17%)
  - ✓ Increases turn-on current overshoot (40%-> 57%)



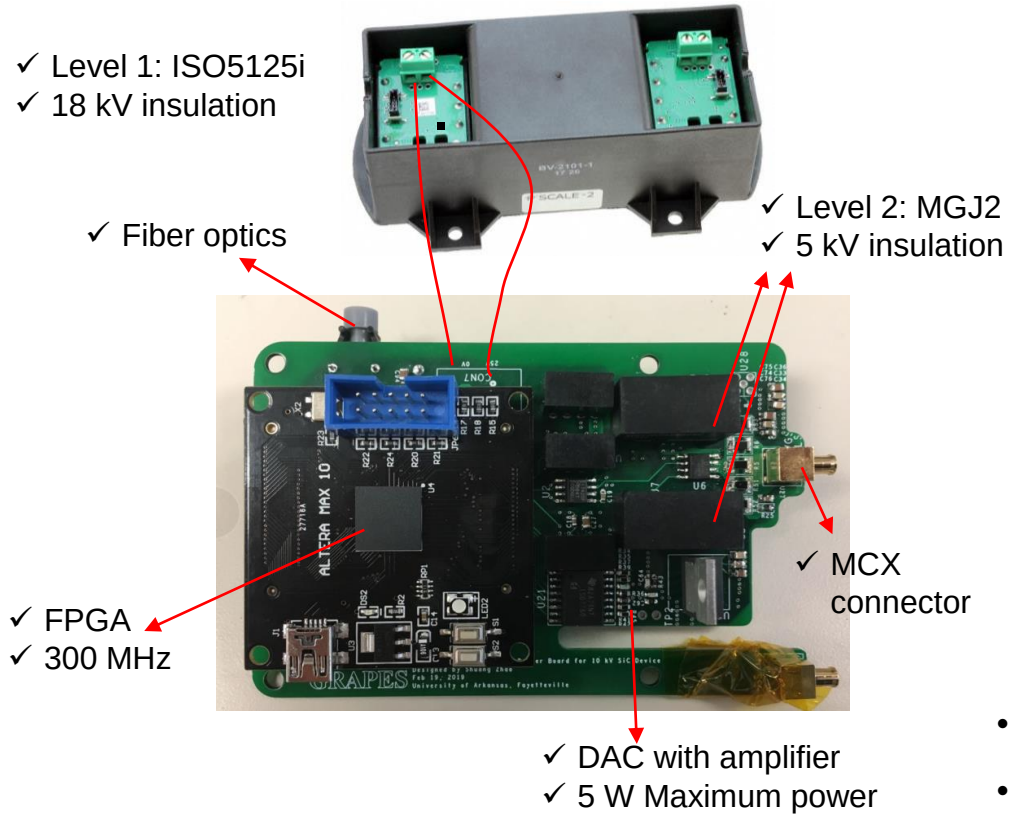
- Slower turn-on mode
  - ✓ Increase turn-on losses
  - ✓ Reduce turn-on current overshoot



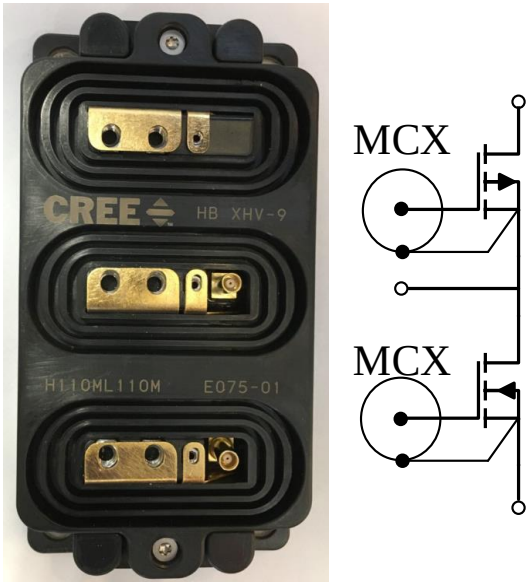
- Slower turn-off mode
  - ✓ Increase turn-off losses
  - ✓ Reduce turn-off voltage overshoot

What fancier stuff can we make? – AGD for 10 kV SiC MOSFET

- Designed PCB – For 10 kV SiC MOSFET



Active gate driver for 10 kV module

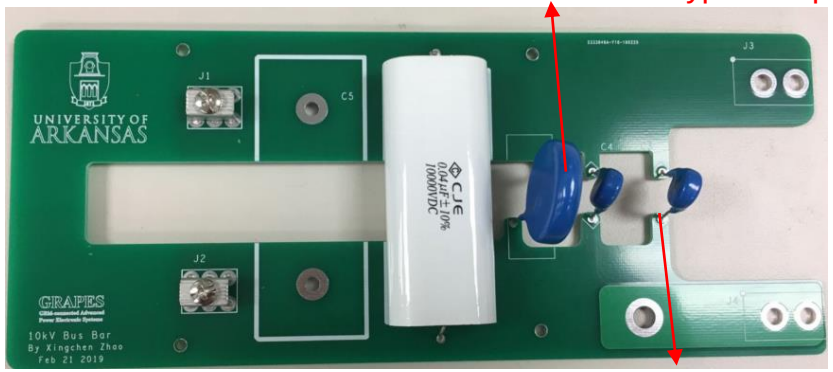


- Online adjustment
- Adaptive control for the slew rate
- Same performance in control and circuitry with 1.2 kV version

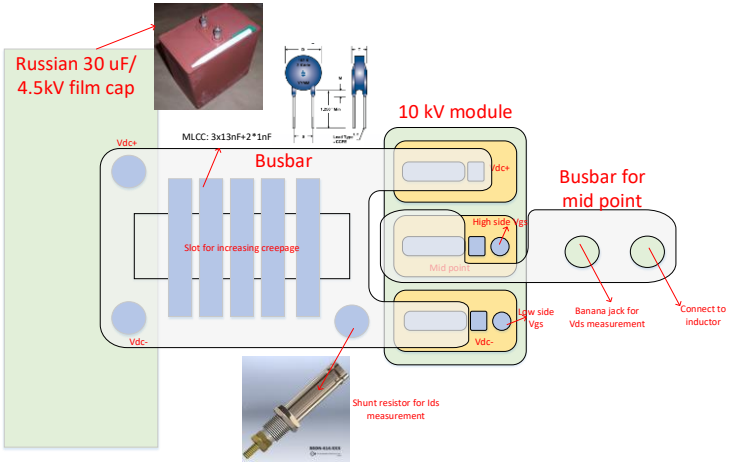
Active Current Sharing Methodologies

- Designed bus bar – For 10 kV SiC power MOSFET

✓ Use 15 kV MLCC as the dc bypass caps

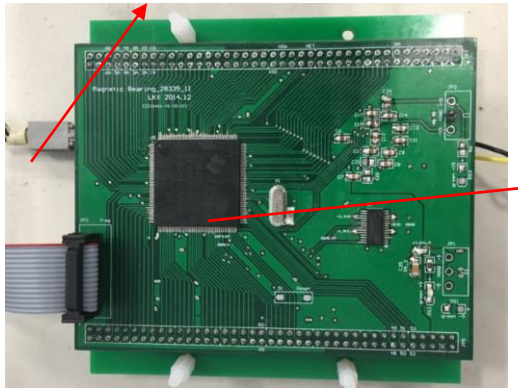


✓ Distance follow MIL 60664-1 standard



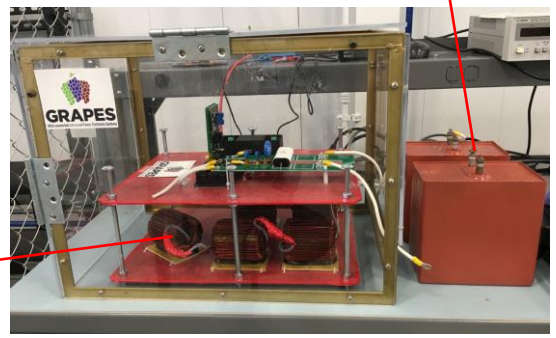
- DSP controller with the fiber transmitter

✓ Fiber transmitter



✓ DSP: 28335

✓ 30/2 μF

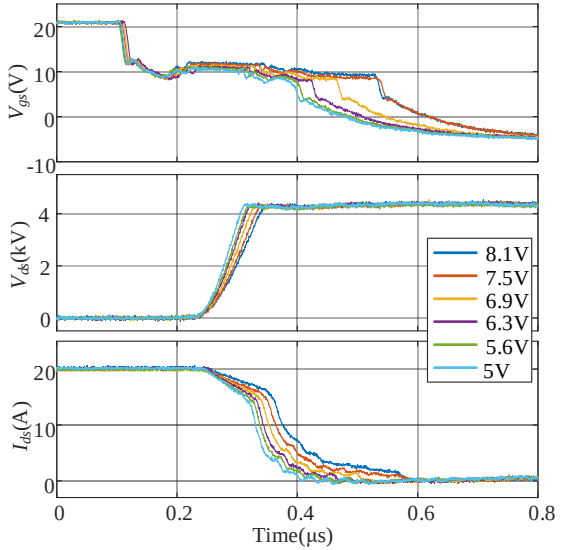


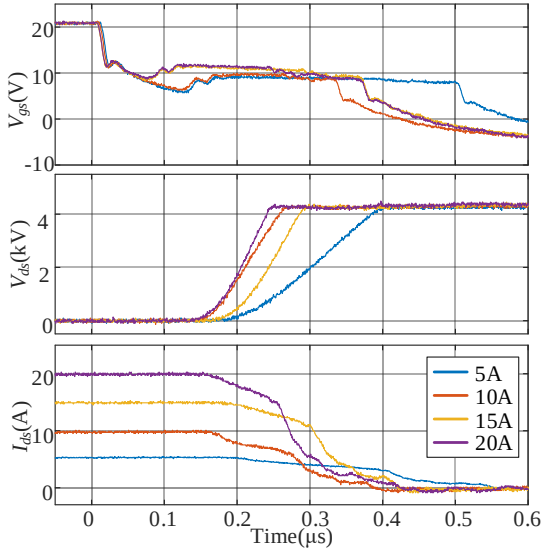
✓ 1.2x5 mH

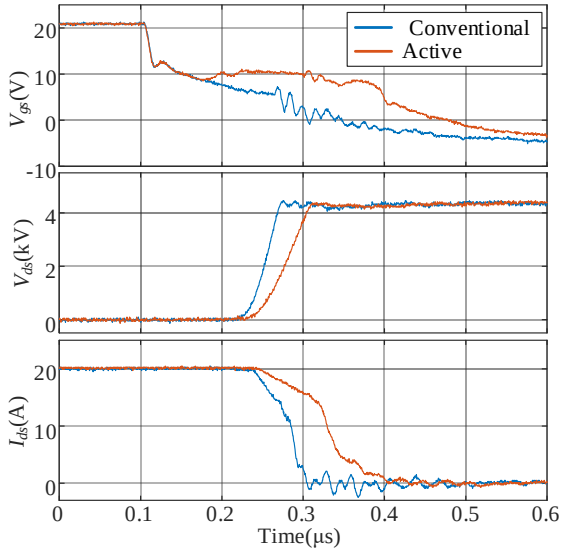
10 kV double pulse test setup

Active Current Sharing Methodologies

- Experimental verification on 10 kV devices







- Comparison of slower turn-off with different V_{int}

V_{int}	dv/dt(V/ns)
Conventional	94.78
5 V	58.8
5.6 V	54.32
6.3 V	52.4
6.9 V	49.16
7.5 V	43.56
8.1 V	40.37

- Comparison of slower turn-off with different I_O, (V_{int} = 7.2 V)

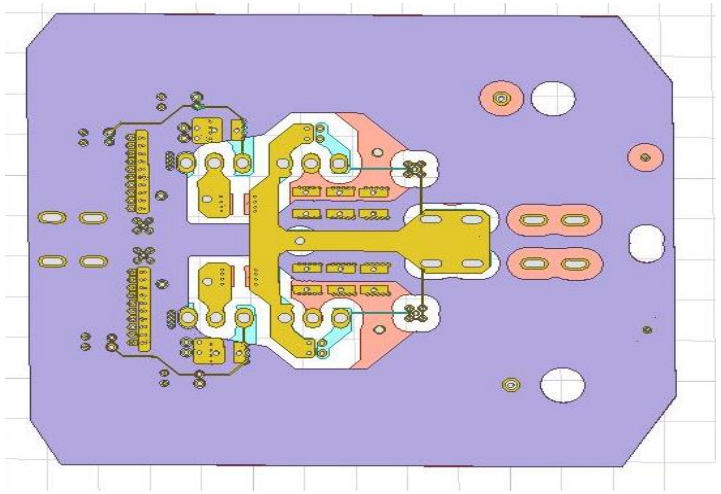
V_{int}	Energy losses
Conventional	2302 μJ
5 V	4384 μJ
5.6 V	4629 μJ
6.3 V	4977 μJ
6.9 V	5555 μJ
7.5 V	6259 μJ
8.1 V	7410 μJ

- Comparison of CGD with AGD

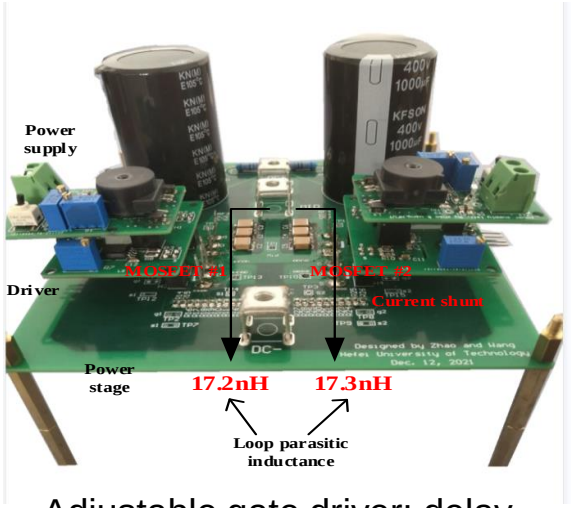
V_{int}	di/dt(A/ns)
Conventional	0.34
5 V	0.158
5.6 V	0.145
6.3 V	0.138
6.9 V	0.122
7.5 V	0.109
8.1 V	0.097

Active Current Sharing Methodologies

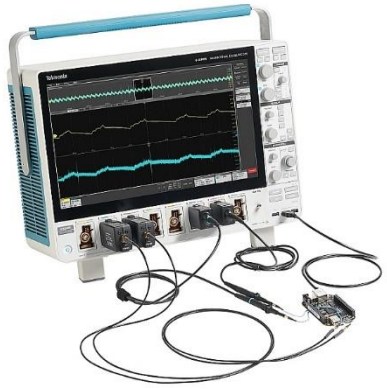
Does that work on current sharing? – Try!



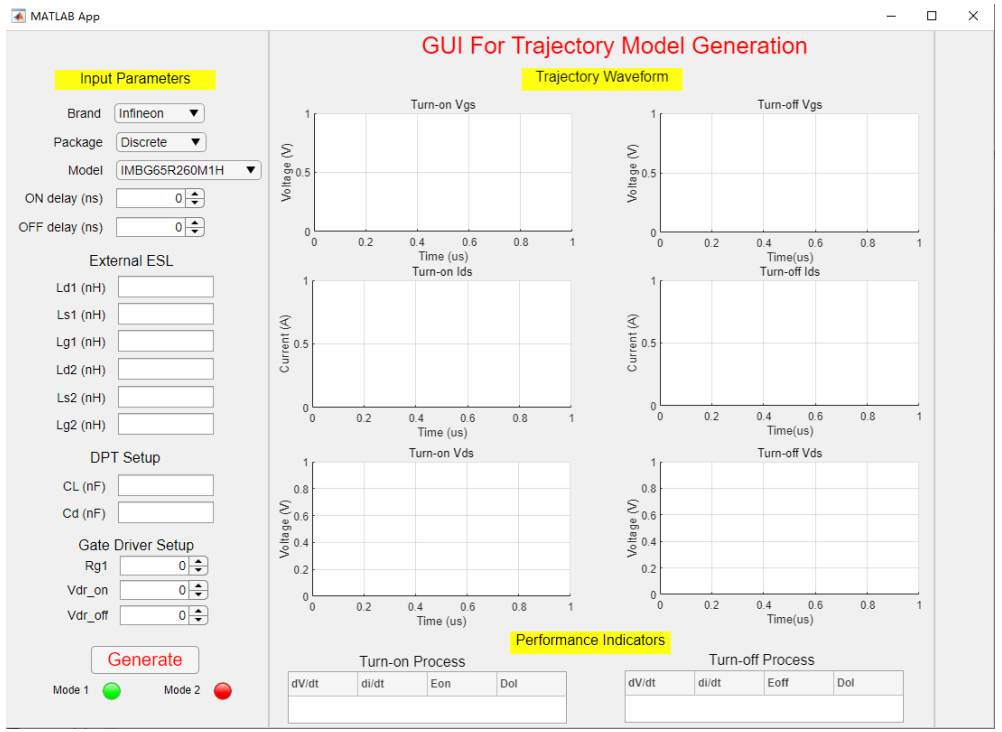
ANSYS-assisted layout design



Adjustable gate driver: delay time + driver voltage



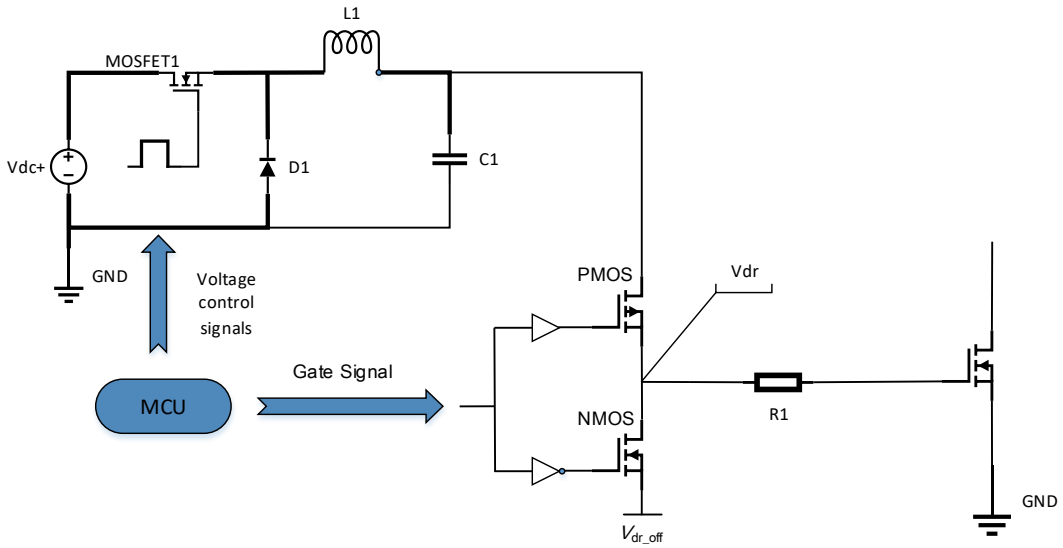
Tek 500MHz 8-channels oscope



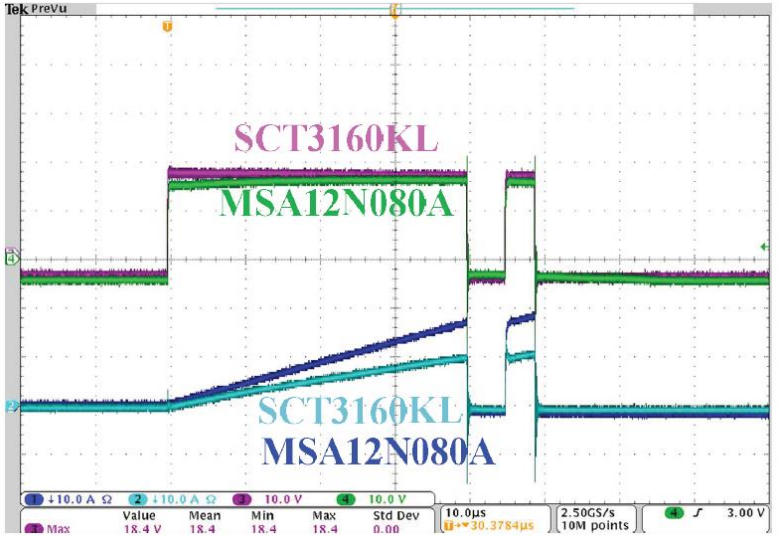
GUI for paralleling MOSFET modeling

Active Current Sharing Methodologies

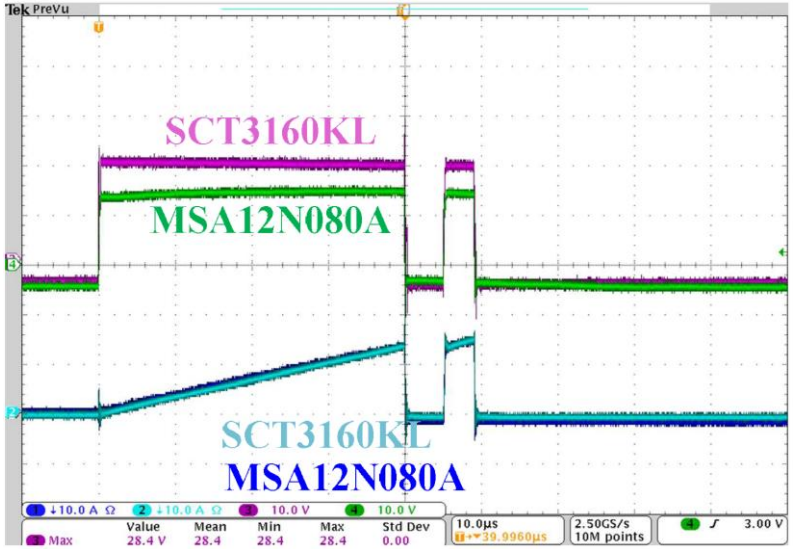
- With adjustable Vdr for static balance



Circuit schematics of adjustable Vdr AGD



Without active gate driver

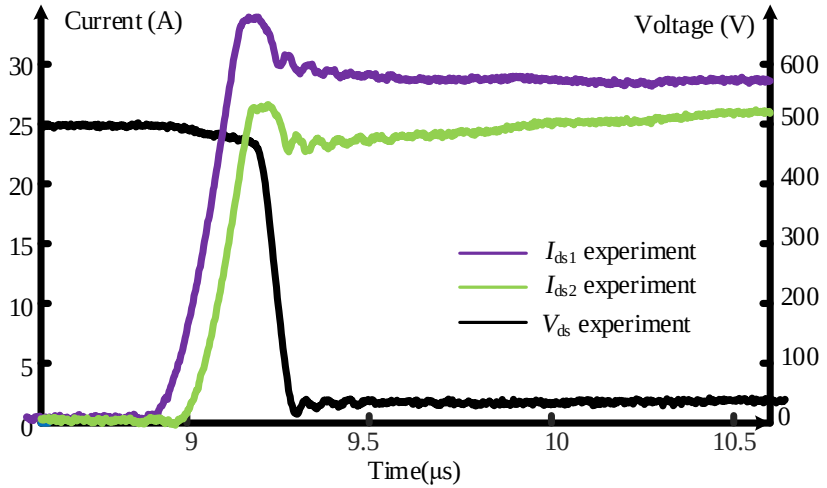


With active gate driver

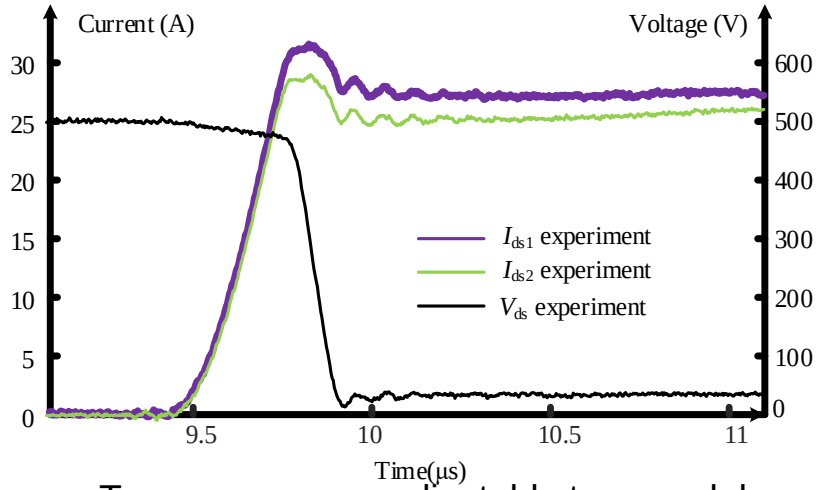
Y. Wei, L. Du, X. Du and A. Mantooth, "Multi-level active gate driver for SiC MOSFETs with paralleling operation," in *Proc. Workshop Control Modelling Power Electron. (COMPEL)*, Cartagena, Colombia, Dec. 2021.

Active Current Sharing Methodologies

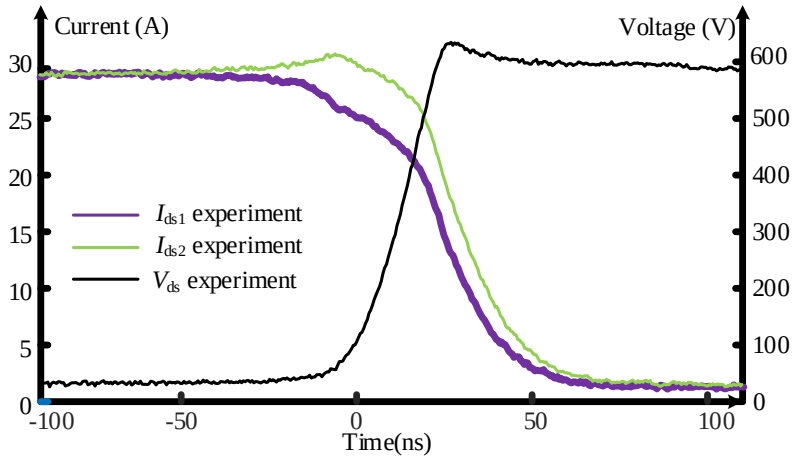
- With adjustable delay time gate driver for transient balance



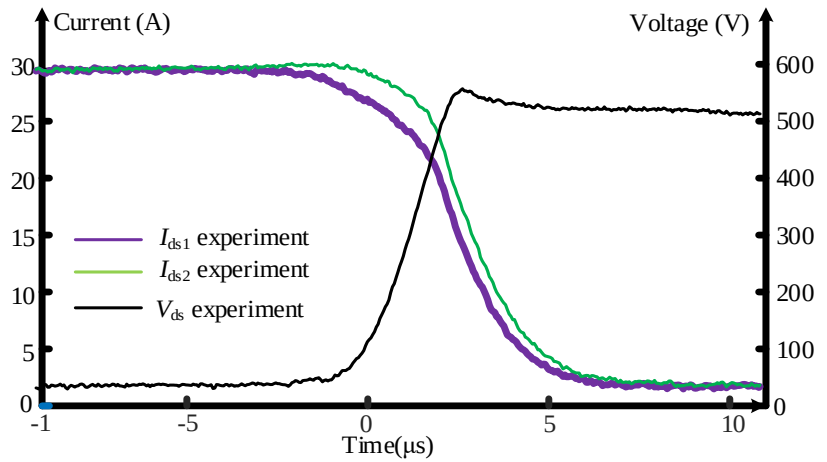
Turn-on process



Turn-on process: adjustable turn-on delay

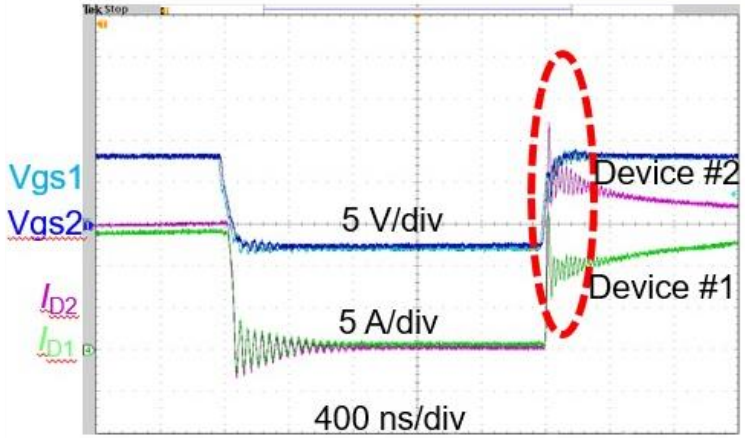


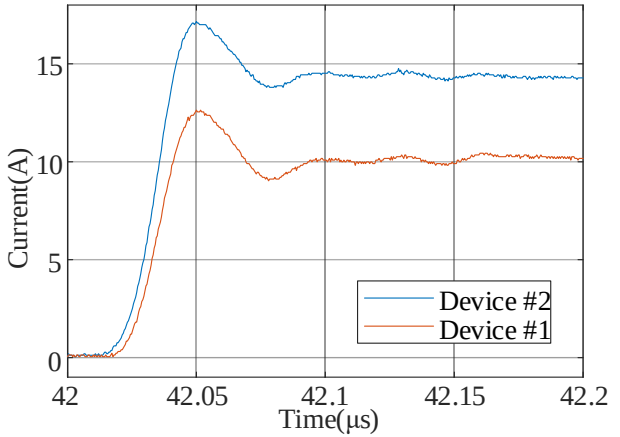
Turn-off process



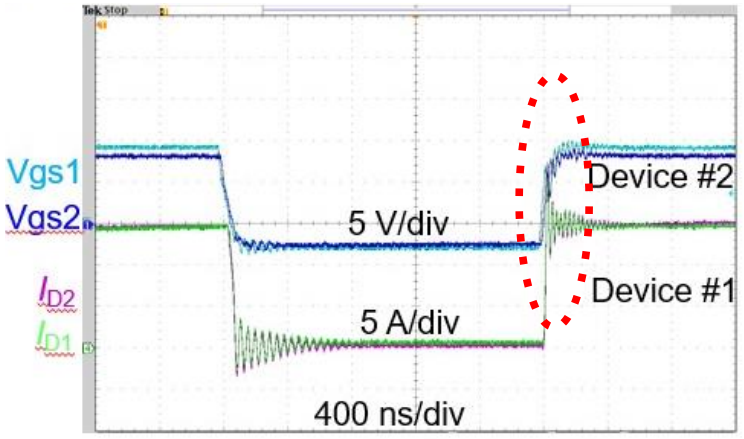
Turn-off process: adjustable turn-on delay

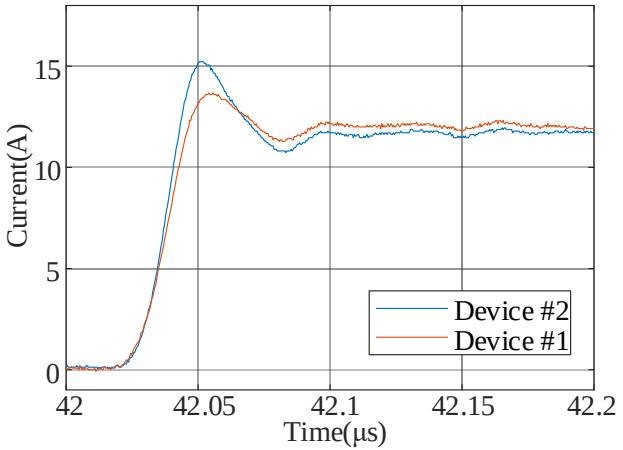
- With adjustable V_{dr} for transient balance





Turn-on process without AGD





Turn-on process with AGD

Part II – Active Current Sharing Methodologies

03

Conclusions and insight

Conclusions and Insight

❑ Conclusions

Current sharing solutions

Power module:
- preselection of chips
- optimization of package layout
- Optimization of PCB/bus bar layout

External passives:
- L/C/R
- Hybrid

Driver-based:
- Static – Only change Vdr
- Five adjustable freedoms

MICROCHIP

Microchip AgileSwitch AGD

❑ Insight

Challenges for external passives:

- ❑ Higher cost -> Commercialization
- ❑ Longer power loop can increase the parasitics
- ❑ Higher impedance can reduce the system efficiency

Challenges for AGD-based:

- ❑ Higher cost and complicated circuitry -> Struggling for commercialization
- ❑ Very fast switching transient of SiC -> Difficult for Feedback control and timing sequence design

Optimization of the power device/module:

- ❑ Preselection of chips + circuit layout optimization: Still the most preferred solution in the industry
- ❑ Automatic layout generation tools needed in the future

Publications

[1]H. Li, S. Munk-Nielsen, X. Wang, R. Maheshwari, S. Beczkowski, C. Uhrenfeldt, W.-Toke Frank, ‘Influences of Device and Circuit Mismatches on Paralleling Silicon Carbide MOSFETs’, IEEE Transaction on Power Electronics, Vol.31, No.1, pp:621 - 634, Jan.2016.

[2]H. Li, S. Munk-Nielsen, S. Beczkowski, X. Wang, ‘A novel DBC layout for current imbalance mitigation in SiC MOSFET multichip power modules’, IEEE Transaction on Power Electronics, vol. 31, no. 12, pp. 8042-8045, Dec.2016.

[3]H. Li, S. Munk-Nielsen, X. Wang, S. Beczkowski, S. Jones, X. Dai, ‘Effects of Auxiliary-Source Connection in Multichip Power Modules’, IEEE Transaction on Power Electronics, Vol.32, No.10, pp:7816 - 7823, Oct.2017.

[4] H. Li, W. Zhou, X. Wang, S. Munk-Nielsen, D. Li, Y. Wang, X. Dai, ‘Influence of Paralleling dies and Paralleling Half Bridges on Transient Current Distribution in Multichip Power Modules’ IEEE Transaction on Power Electronics, Vol.33, No.8, pp:6483 - 6487, Aug.2018.

[5] H. Li and S. Munk-Nielsen, "Challenges in Switching SiC MOSFET without Ringing," PCIM Europe, 2014, pp. 1-6.

[6] H. Li, C. Zhu, P. Mumby-Croft, D. Li, Y. Wang and X. Dai, "Influence of Auxiliary Gate and Emitter Connections on Short Circuit Behaviour of Multichip IGBT Modules," PCIM Europe, 2018, pp. 1-5.

[7] H. Li, S. Munk-Nielsen, C. Pham and S. Bęczkowski, "Circuit mismatch influence on performance of paralleling silicon carbide MOSFETs," 2014 16th European Conference on Power Electronics and Applications, 2014, pp. 1-8.

[8] Helong Li and S. Munk-Nielsen, "Detail study of SiC MOSFET switching characteristics," 2014 IEEE 5th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2014, pp. 1-5.

[9] N. Baker, F. Iannuzzo and H. Li, "Impact of Kelvin-Source Resistors on Current Sharing and Failure Detection in Multichip Power Modules," *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, 2018, pp. 1-7.

[10]H. Li, S. Beczkowski, S. Munk-Nielsen, R. Maheshwari and T. Franke, "Circuit mismatch and current coupling effect influence on paralleling SiC MOSFETs in multichip power modules," *Proceedings of PCIM Europe,* 2015, pp. 1-8.

Publications

[11] S. Zhao, X. Zhao, A. Dearien, Y. Wu, Y. Zhao, and H. A. Mantooth, “An intelligent versatile active gate driver for high-voltage SiC MOSFET and its optimization,” *IEEE J. Emer. Sel. Topics Power Electron*., vol. 8, no. 1, pp. 429-441, Jun. 2020

[12] S. Zhao *et al*., "Adaptive multi-level active gate drivers for SiC power devices," *IEEE Transaction on Power Electronics*., vol. 35, no. 2, pp. 1882-1898, Feb 2020.

[13] S. Zhao, X. Zhao, Y. Wei, Y. Zhao and H. A. Mantooth, "A review on switching slew rate control for silicon carbide devices using active gate drivers*," IEEE J. Emerg. Sel. Topics Power Electron*., vol. 9, no. 4, pp. 4096-4114, Jul. 2020.

[14] S. Zhao, A. Kempitiya, W. T. Chou, V. Palija and C. Bonfiglio, "Variable dc-link voltage LLC resonant DC/DC converter with wide bandgap power devices," *IEEE Transactions on Industry Applications*, vol. 58, no. 3, pp. 2965-2977, Feb. 2022.

[15] A. Dearien, S. Zhao, C. Farnell, and H. A. Mantooth, “Active slew rate control for SiC power MOSFETs using gate resistance vs. intermediate voltage level,”in Proc. Int. Conf. Power. Electron.(ICPE-ECCE Asia), Busan, Korea, 2019.

[16] S. Zhao, H. A. Mantooth, A. Dearien, An intelligent multi-level active gate driver for SiC power MOSFET, US11277127B1, Feb. 2022

[17] S. Zhao and W. Chou, "Analytic Model of the Voltage Oscillation in a Power Conversion System with DC-Link Capacitors," 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021, pp. 5554-5560.

[18] S. Zhao, M. Zhang, H. Li, A kind of SiC MOSFET switching waveform regaining method based on the switching trajectory model (Pending China Patent, 2022)

[19] S. Zhao, C. Wang, H. Li, L. Ding, A kind of current measurement system for paralleling SiC MOSFET current, (Pending China Patent, 2022)

[20] M. Zhang, S. Zhao, H. Li, L. Ding, Trajectory-Model-Based Switching Waveform Restoration Method for Accurate Dynamic Characterization of SiC Power MOSFET, in Proc. PEAC, Guangzhou, China, 2022 (Accepted)

[21] C. Wang, S. Zhao, L. Ding, Analytical Model of the Parallel-Connected Silicon Carbide MOSFET Switching Behavior Under Asynchronous Gate Signals, in Proc. ITEC-AP, Haining, Zhejiang, China, 2022 (Accepted)

Parallel-Connected SiC MOSFETs – Essence, Challenges, and Solutions

Thanks!

shuang.zhao@hfut.edu.cn

shuang.zhao@ieee.org