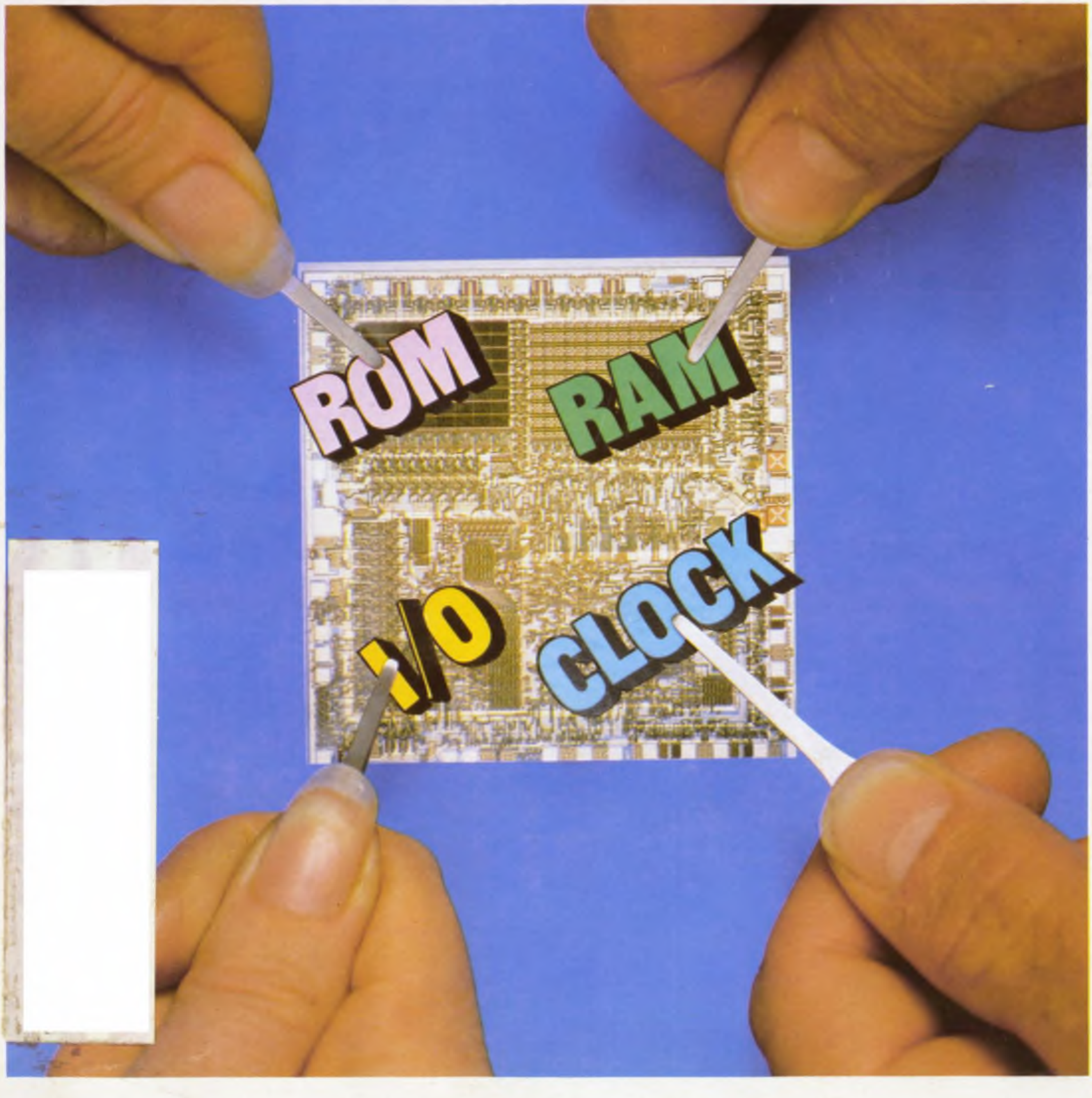
VOL. 25 NO. 14

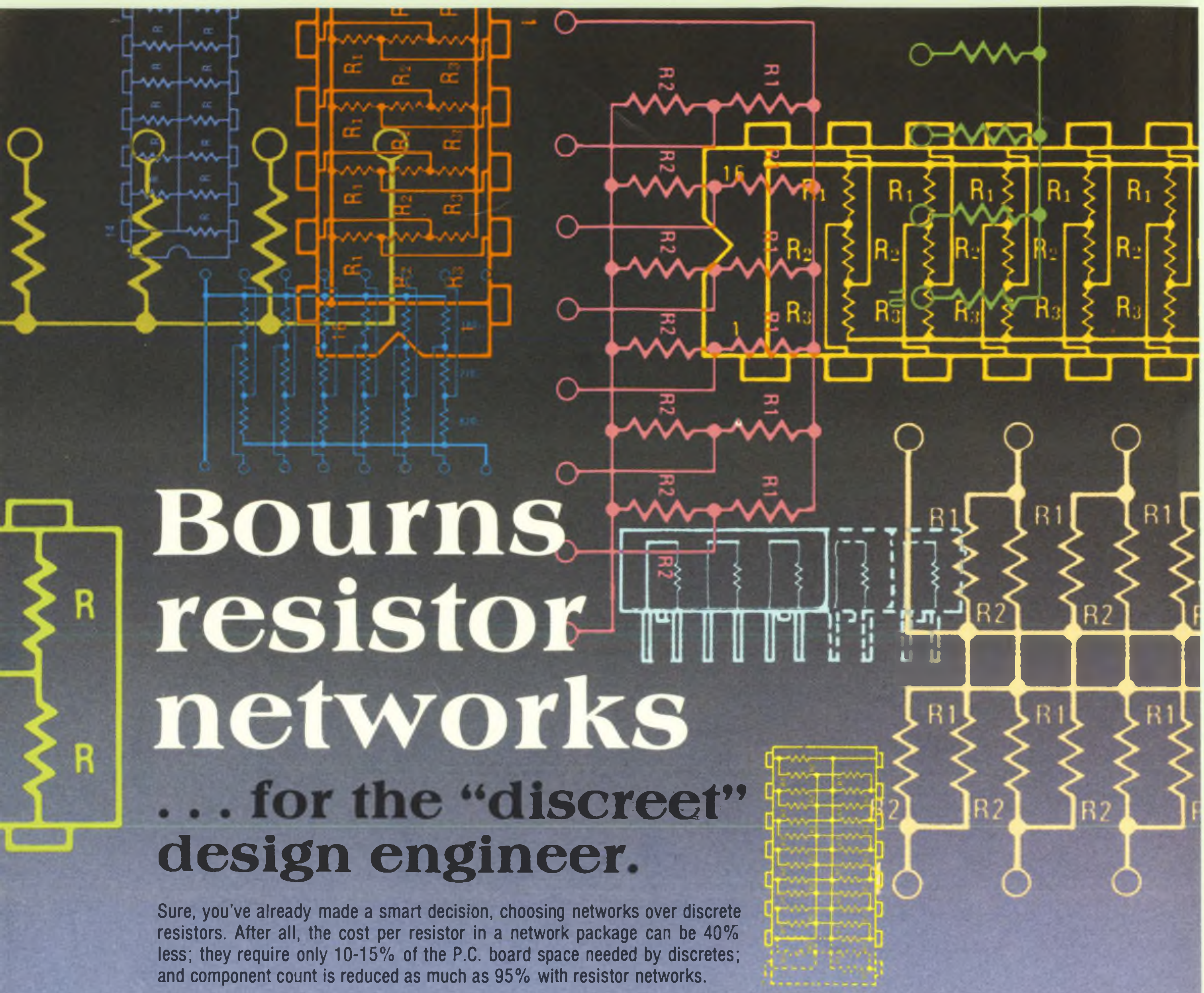
# Electronic Design®

FOR ENGINEERS AND ENGINEERING MANAGERS

JULY 5, 1977

**A complete μC on a chip?** It's getting closer, with most major functions now combined on a single die. Newer technologies are making the μP itself more powerful, providing higher speeds and larger instruction sets. Even UV PROMs can be put on the same chip. For the latest μP developments turn to page 26.





# Bourns resistor networks

## . . . for the "discreet" design engineer.

Sure, you've already made a smart decision, choosing networks over discrete resistors. After all, the cost per resistor in a network package can be 40% less; they require only 10-15% of the P.C. board space needed by discretes; and component count is reduced as much as 95% with resistor networks.

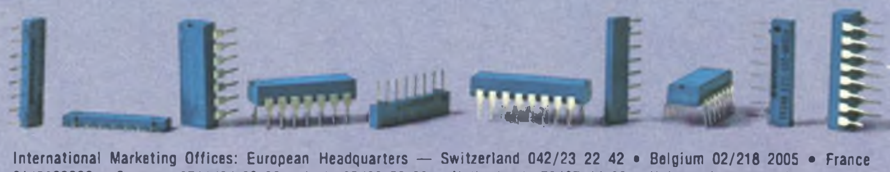
But, when choosing a network supplier, you should also consider these points:

1. Bourns has the broadest network product line in the industry — over 1000 part numbers in all. And our standard DIP circuits range from simple pull-up configurations to Thevinin-equivalent ECL terminators and memory interface circuits.
2. Bourns Krimp-Joint™ offers both a mechanical and electrical bond that lap or butt joint construction doesn't provide. The lead is crimped onto the network element and a high-temp, reflow-resistant solder is used to prevent failure during wave soldering and in circuit thermal cycling and vibration.
3. Bourns was the first manufacturer to offer a complete line of off-the-shelf, super low profile SIPs with demonstrated automatic insertion capability.

These are the facts. So, now you can be even more "discreet". We're sure you'll specify Bourns Resistor Networks — direct or through your local distributor.

Send today for our new 1977 Resistor Networks Catalog.

TRIMPOT PRODUCTS DIVISION, BOURNS, INC., 1200 Columbia Avenue, Riverside, CA 92507, Telephone 714 781-5415 — TWX 910 332-1252.



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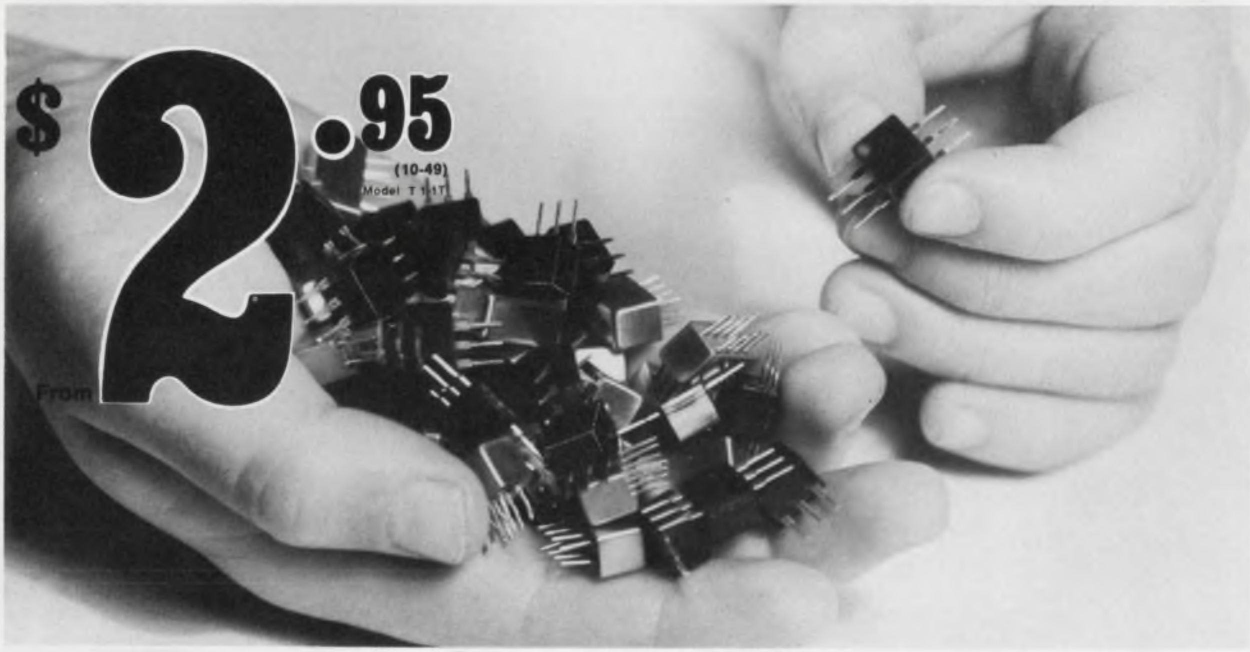
**For Immediate Application — Circle 130**
**For Future Application — Circle 230**

# RF TRANSFORMERS




# Have it your way!

## 36 models to choose from, 10KHz-800MHz

It costs less to buy Mini-Circuits wideband RF transformers. The T-series (plastic case) and TMO series (hermetically sealed metal case) RF transformers operate with impedance levels from 12.5 ohms to 800 ohms and have low insertion loss, 0.5 dB typ. High reliability is associated with every transformer. Every production run is 100% tested, and every unit must pass our rigid inspection and high quality standards. Of course, our one-year guarantee applies to these units.

**DC ISOLATED PRIMARY & SECONDARY**

N×50 Ω / 50 Ω

| Model | | | | | | |
|---|---|---|---|---|---|---|
| Metal Case | TMO 1-1 | TMO 1.5-1 | TMO 2.5-6 | TMO 4-6 | TMO 9-1 | TMO 16-1 |
| Plastic Case | T 1-1 | T 1.5-1 | T 2.5-6 | T 4-6 | T 9-1 | T 16-1 |
| Freq Range, MHz | .15-400 | .1-300 | .01-100 | .02-200 | .15-200 | .3-120 |
| Impedance Ratio | 1 | 1.5 | 2.5 | 4 | 9 | 16 |
| Max. Insertion Loss | MHz | MHz | MHz | MHz | MHz | MHz |
| 3 dB | .15-400 | 1-300 | .01-100 | 02-200 | .15-200 | .3-120 |
| 2 dB | .35-200 | .2-150 | .02-50 | 05-150 | .3-150 | .7-80 |
| 1 dB | 2-50 | .5-80 | .05-20 | 1-100 | 2-40 | 5-20 |
| Price, Model TMO | $4.95 | $6.25 | $5.95 | $5.95 | $5.45 | $5.95 |
| (10-49) Model T | $2.95 | $3.95 | $3.95 | $3.95 | $3.45 | $3.95 |

**UNBALANCED PRIMARY & SECONDARY**

50 Ω / N×50 Ω

| Model | | | | | |
|---|---|---|---|---|---|
| Metal Case | TMO 2-1 | TMO 3-1 | TMO 4-2 | TMO 8-1 | TMO 14-1 |
| Plastic Case | T 2-1 | T 3-1 | T 4-2 | T 8-1 | T 14-1 |
| Freq Range, MHz | 015-600 | .5-800 | 5-600 | .15-250 | .2-150 |
| Impedance Ratio | 2 | 3 | 4 | 8 | 14 |
| Max. Insertion Loss | MHz | MHz | MHz | MHz | MHz |
| 3 dB | 015-600 | 5-800 | 2-600 | 15-250 | .2-150 |
| 2 dB | .02-400 | 2-400 | 5-500 | 25-200 | 5-100 |
| 1 dB | 05-200 | | 2-250 | 2-100 | 2-50 |
| Price, Model TMO | $5.45 | $6.25 | $5.45 | $5.45 | $6.25 |
| (10-49) Model T | $3.45 | $4.25 | $3.45 | $3.45 | $4.25 |

**DC ISOLATED PRIMARY & SECONDARY CENTER-TAP SECONDARY**

N×50 Ω / 50 Ω

| Model | | | | | | | |
|---|---|---|---|---|---|---|---|
| Metal Case | TMO 1-1T | TMO 2-1T | TMO 2.5-6T | TMO 3-1T | TMO 4-1 | TMO5-1T | TMO 13-1T |
| Plastic Case | T 1-1T | T 2-1T | T 2.5-6T | T 3-1T | T 4-1 | T 5-1T | T 13-1T |
| Freq Range, MHz | 05-200 | .07-200 | .01-100 | .05-250 | 2-350 | .3-300 | .3-120 |
| Impedance Ratio | 1 | 2 | 2.5 | 3 | 4 | 5 | 13 |
| Max. Insertion Loss | MHz | MHz | MHz | MHz | MHz | MHz | MHz |
| 3 dB | 05-200 | 07-200 | 01-100 | .05-250 | .2-350 | 3-300 | .3-120 |
| 2 dB | .08-150 | .1-100 | .02-50 | .1-200 | 35-300 | 6-200 | .7-80 |
| 1 dB | 2-80 | 5-50 | 05-20 | 5-70 | 2-100 | 5-100 | 5-20 |
| Maximum Amplitude Unbalance MHz | | | | | | | |
| .1 dB | 5-80 | 1-50 | .1-20 | 1-70 | 5-100 | 10-100 | 5-20 |
| .5 dB | .05-200 | 07-200 | .01-100 | 05-250 | 2-350 | .3-300 | 3-120 |
| Maximum Phase Unbalance Degrees MHz | | | | | | | |
| 1° | 5-80 | 1-50 | 1-20 | 1-70 | 5-100 | 10-100 | 5-20 |
| 5° | 05-200 | .07-200 | .01-100 | 05-250 | 2-350 | .3-300 | .3-120 |
| Price (10-49) | | | | | | | |
| Model TMO | $5.95 | $6.25 | $6.25 | $5.95 | $4.95 | $6.25 | $6.25 |
| Model T | $3.95 | $4.25 | $4.25 | $3.95 | $2.95 | $4.25 | $4.25 |

Primary Impedance: 50 ohms
Total Input Power: ¼ watt

| | TMO-series | T-series |
|---|---|---|
| | .25 cu. inches | 02 cu. inches |
| | .07 ounces | .01 ounces |

### Designers Kit Available

**(TK-1)** — 2 transformers of each type T1-1, T2-1, T4-1, T9-1, T16-1 **$32.00**

**(TMK-2)** — 2 transformers of each type TMO1-1, TMO2-1, TMO4-1, TMO9-1, TMO16-1 **$49.50**

**WE'VE GROWN** *Customer acceptance of our products has been so overwhelming, we've been forced to move to larger facilities — THANKS.*

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**CIRCLE NUMBER 3**

VOL. 25 NO. 14

# Electronic Design®

FOR ENGINEERS AND ENGINEERING MANAGERS

JULY 5, 1977

## NEWS



## TECHNOLOGY



## PRODUCTS



## DEPARTMENTS



**Cover:** Photo by Rob Janoff, courtesy of Intel

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# Across the desk

## The real difference is management

Ulrich Rohde's opinions on European and American engineers (ED No. 24, Nov. 22, 1976, p. 96) are not fair to the engineers in West Germany. Knowing from my own experience the American *and* German way to running companies in the electronics field, the blame lies with company management for long design times, cost overruns, lack of teamwork, lack of realism and so on. If German engineers are lined up according to the rules of American management, they will obtain the same results as Americans. It's as simple as that. The differences in their educational backgrounds are not nearly as great as Mr. Rohde implies; moreover, education is of questionable value in such a fast-moving area.

Some other erroneous remarks in Mr. Rohde's article ought to be commented upon. There is no such thing as an "engineers' union" in Germany, much less a strong one. Also, a simple letter is usually sufficient to fire an engineer; there are some restrictions as far as older people are concerned. And as far as "excellence" in electronics products is concerned, I find this excellence mostly—apart from some noteworthy exceptions—in U.S. products. The five-year old technological gap is liable to increase rather than shrink.

Far and away, the years I worked as a manager in an American electronics firm have been the best ones in my professional life and I am grateful that I was given the opportunity to experience the difference. It's like after eating the proverbial apple: You are never the same any more.

*Artur Seibt*
*Engineer*

8501 Schwaig
Handelstrasse 28
West Germany

## Ulrich Rohde replies

I have to disagree with Mr. Seibt for the following reasons:

1. Working procedures in large companies are a joined agreement between union representatives and management. However, a system can never be better than the interest of the individuals.
2. Since the fast-moving areas are mainly a question of technology and computers, in-depth training is of utmost importance.
3. In certain states of Germany, union contracts cover jobs, including positions like lab leaders or project managers. Because of equal-opportunity employment regulations, the union can prevent both the hiring and firing of engineers, regardless of age.
4. In my opinion, the best combination would be a German research team, an American project-design team and an American manufacturing and marketing manager.

## Misplaced Caption Dept.

Mother was right. You shouldn't date an engineer right after work.

Sorry. That's Edward Hopper's "Automat," which hangs in the Des Moines Art Center, IA.

**Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Managing Editor, Electronic Design, 50 Essex St., Rochelle Park, NJ 07662. Try to keep letters under 200 words. Letters must be signed. Names will be withheld upon request.**

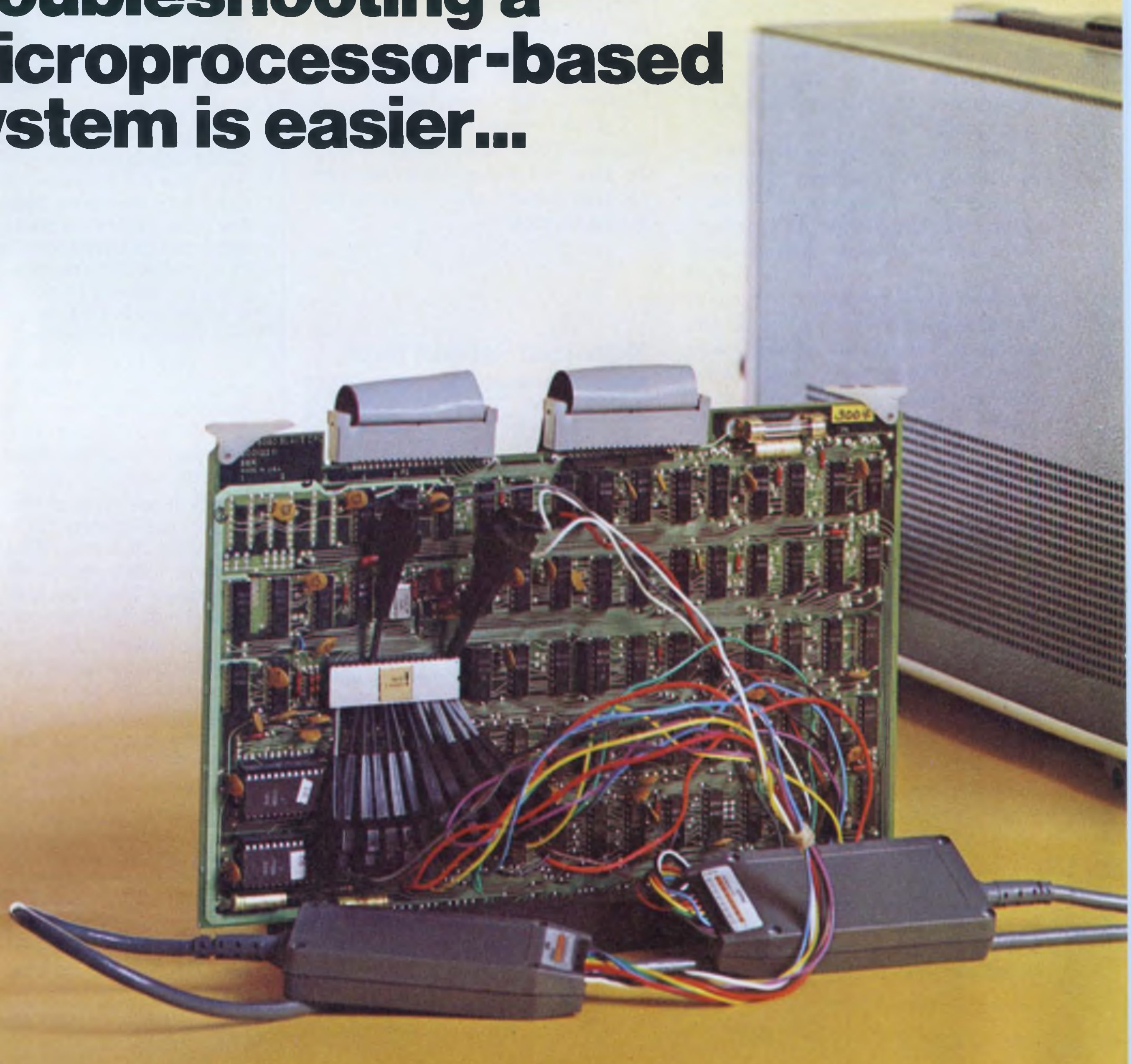
You've designed, debugged, and loaded your system software. Now you need several powerful capabilities to ensure trouble-free execution on the prototype: the ability to look at data in different ways . . . to compare known good data with new data quickly and easily . . . to analyze both system and peripheral-interface timing.

The TEKTRONIX 7D01F Logic Analyzer offers you all those capabilities in a single instrument.

**Look at data in different ways.**

The 7D01F lets you choose from five display modes: maps; state tables in hexadecimal, binary, or octal code; or timing diagrams. How often have you encountered a problem you knew you could spot just by scanning overall program flow? How often have you wished you could compare state tables in the hexadecimal code you work with as well as the binary code your microprocessor knows? How often have you wanted to switch from a state table display to its corresponding timing diagram? The 7D01F can help at each step of this troubleshooting procedure.

# Troubleshooting a microprocessor-based system is easier...



**Compare known good data with new data.**

The 7D01F features two comparison modes which facilitate in-depth software/hardware debugging. The EXCLUSIVE-OR and RESET-IF modes speed up what would otherwise be a very tedious process: checking the program flow chart against what falls out when the program is run.

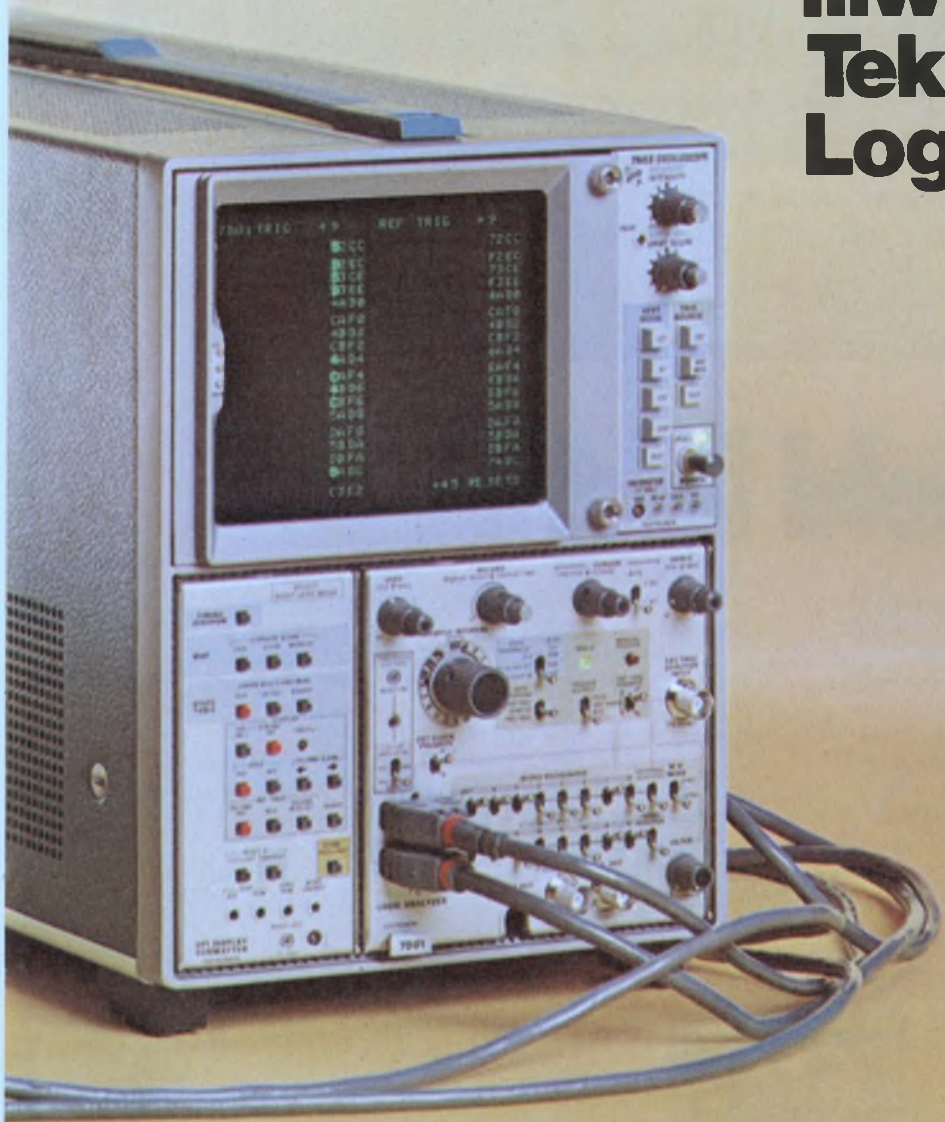
For an EXCLUSIVE-OR comparison, simply verify known good data, store it in reference memory; acquire new data, and select a table comparison mode. The reference table and the compared table (which may be in hex, octal, or binary) will be displayed side by side, and the differences between the two will be highlighted for ready identification.

Use RESET-IF to track down an intermittent fault. In this mode the 7D01F can automatically acquire and compare up to 4096 bits of new data to 4096 bits of reference data. Data is continually reacquired until a mismatch occurs. If there is a mismatch, the instrument holds the display, highlights the differences, and displays the number of resets that occurred. This frees the operator from continually monitoring for wandering programs, intermittent loops, or ragged-edge timing problems.

**Analyze system and interface timing.**

The 7D01F offers synchronous data acquisition at speeds up to 50 MHz. But it is sometimes necessary to view microprocessor operation with increased timing resolution, as well as to locate timing discrepancies in the system's interface with the outside world. You may, for example, need to asynchronously examine data coming into the I/O port before you can determine whether incorrect information is coming from the I/O port itself or the hardware on the other side. The 7D01F offers asynchronous data acquisition at sample intervals of up to 100 MHz.

# ...with the Tektronix 7D01F Logic Analyzer.



All these unique features are available only in the TEKTRONIX Logic Analyzer. To find out more about how the 7D01F can simplify your work with microprocessor-based systems, just call your local Tektronix Field Engineer. He'll demonstrate the 7D01F in your application, and acquaint you with its many other features, including 16-channel word recognition, 1MΩ/5 pf logic probes, 16-channel data acquisition, 4k formattable memory, and 7000-Series mainframe compatibility.

You should also send for our newest application note, describing in detail how a 7D01F can be used with microprocessor-based systems. Write Tektronix, Inc., P.O. Box 500, Beaverton, Oregon 97077. In Europe, write Tektronix Limited, P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

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**For technical data circle 6**
**For demonstration circle 7**

# Field lab!

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The SE7000 handles the full range of requirements from routine 14-track midband all the way to 42-track recording capability. It offers a choice of eight speeds between 15/16 and 120 ips providing 600 kHz DR or dc to 80 kHz FM at 120 ips. Equalizers and filters for all tape speeds are built in as standard. And it has a built-in calibration module, eliminating the need for time-consuming cross-patching.

All these features are packed into a transportable unit so rugged that the system is warrantied unconditionally for a full year. Complete with its internal AC or DC power supply, the weight is less than 100 pounds.

The SE7000 has gone into the field in automotive, aerospace, petrochemical and transportation applications all over the world. Applications, like yours, that need laboratory precision but can't be brought to the lab.

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**CIRCLE NUMBER 8**

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Need a 100 nsec., **low-cost precision** comparator with instant DELIVERY? Our CMP-01 is it, **in stock** at all our distributors. Need even BETTER input performance than the CMP-01? Choose the CMP-02! That includes MIL-STD-883A CLASS B parts, too. On the shelf.

If you use LM111 or LM311-type comparators, you can usually use one of our CMP-01's as a pin-for-pin replacement. Of course, you will have to settle for improved performance, such as higher slew rate, faster settling time, higher open loop gain, higher CMMR, and lower offset voltage, offset current, bias current, and tempco's . . . **AND A LOWER PRICE!**

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**CIRCLE NUMBER 14**

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# BIPOLAR MEMORIES


## THE WORLD'S FIRST 4K STATIC BIPOLAR RAM IS READY FOR ACTIVE DUTY.

You can stop gluing your 1K RAMs together.

Fairchild proudly introduces the very first, fully static, 4K Bipolar TTL RAM.

It also happens to be the fastest 4K RAM ever made.

To make matters better, it's available today at good prices from your Fairchild distributor.

What else would you expect from the world's largest supplier of Bipolar Memories?

### FASTER THAN A ROLLING MOS.

If you think that MOS memories roll along at a pretty fast clip, wait till you see our new static Bipolar RAM perform. The new Fairchild 93471 has an incredible $T_{AA}$ of 50ns max, and 25-30ns typical. On top of all that speed, you get Bipolar reliability backed by Fairchild's Walled Emitter Isoplanar™ process.

Also, because our new device is fully static, no special clocking or refresh circuits are required.

### AN INDUSTRY STANDARD IS BORN.

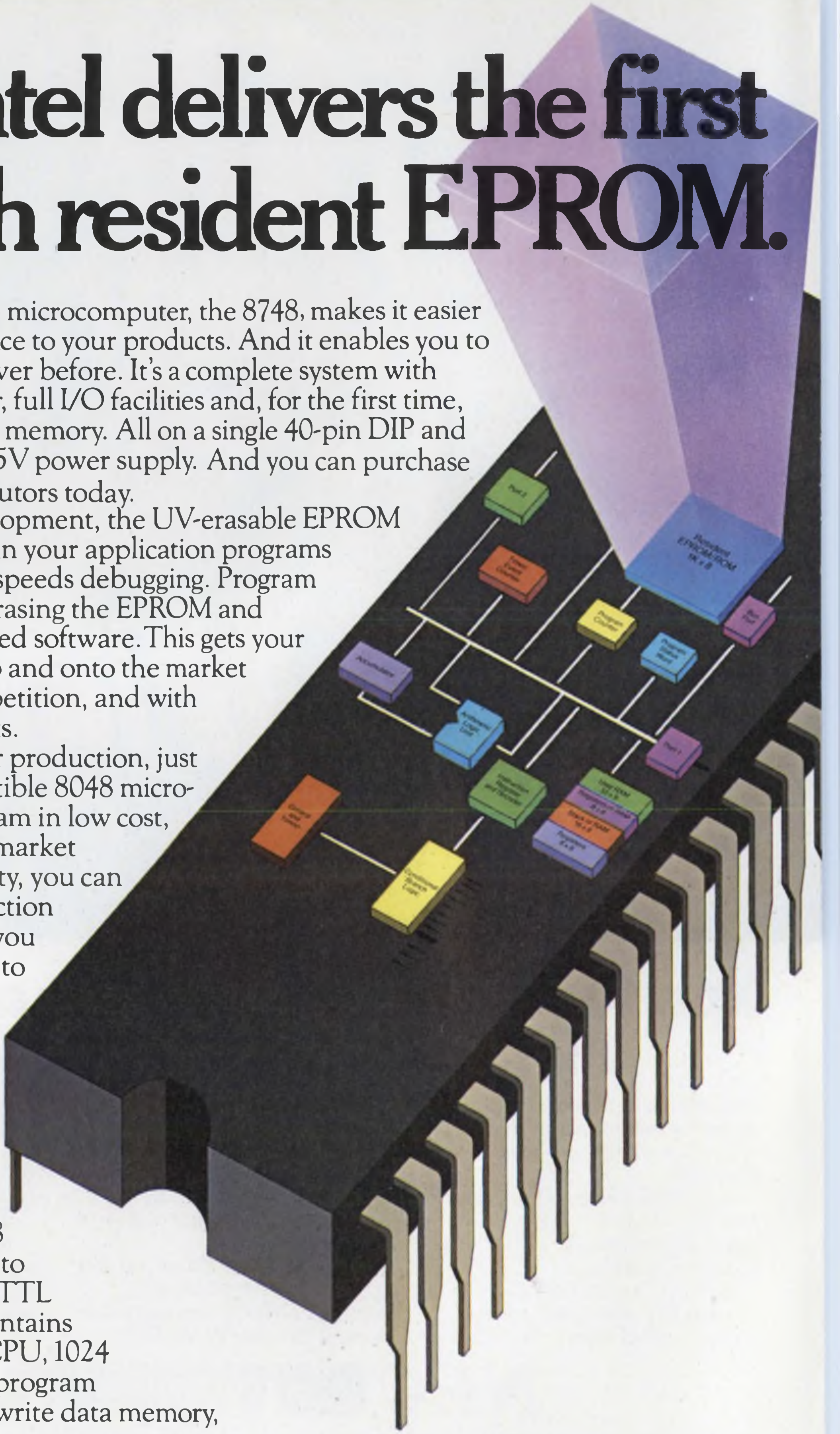
The new 93471 is organized 4096 by one bit. It's a 3-state device in an 18-pin package.

It offers full decoding on the chip, separate data input and data output lines, and active LOW chip select lines.

The power supply is 5 volts with power dissipation 0.12 mW/bit typical. You also get operation over full military and commercial temperature ranges.

The 93471 also comes in a version with an open

# Intel delivers the first with resident EPROM.



Intel's new single chip microcomputer, the 8748, makes it easier than ever to add intelligence to your products. And it enables you to do it at a lower cost than ever before. It's a complete system with powerful central processor, full I/O facilities and, for the first time, resident EPROM program memory. All on a single 40-pin DIP and operating from a single +5V power supply. And you can purchase the 8748 from Intel distributors today.

During product development, the UV-erasable EPROM enables you to load and run your application programs in minutes. The 8748 also speeds debugging. Program changes can be made by erasing the EPROM and reloading with your updated software. This gets your new product out of the lab and onto the market months ahead of the competition, and with reduced development costs.

When you're ready for production, just substitute the fully compatible 8048 microcomputer with your program in low cost, resident masked ROM. If market entry timing has top priority, you can even ship your first production units with the 8748 while you gear up for the switchover to 8048. And by using the 8748 you can respond to non-standard customer requirements without waiting for ROM turn-around.

Intel's advanced MOS/LSI process technology allows a single 8748 or 8048 chip to replace up to 100 or more conventional TTL devices. The 8748/8048 contains an 8-bit general purpose CPU, 1024 bytes of EPROM or ROM program memory, 64 bytes of read/write data memory,

# single chip microcomputer The 8748.

three programmable 8-bit I/O ports, 8 additional control/timing lines, programmable interval timer/event counter, priority interrupts, system clock generator and a full set of system controls. It's a single chip solution to a wide variety of applications, yet it's fully expandable by adding compatible MCS-80™/MCS-85™ I/O chips and Intel® standard memories.

There's also a new 8035 microcomputer that is exactly like the 8748/8048 but without resident program memory. It enables you to precisely match system memory size to your needs, using external ROM or EPROM.

| Part No. | Description | Availability |
|---|---|---|
| | **MCS-48 Components** | |
| 8748 | Single chip μC with 1K bytes EPROM | NOW |
| 8048 | Single chip μC with 1K bytes masked ROM | NOW |
| 8035 | Single chip μC without resident program memory | NOW |
| 8243 | I/O Expander with 16 high current drive I/O lines | NOW |
| 8355 | ROM, 2K bytes, 16 I/O lines | NOW |
| 8155 | RAM, 256 bytes, 22 I/O lines and timer | NOW |
| | **Compatible MCS-80/85 Components** | |
| 2316E | Standard ROM, 2K × 8, 450 ns | NOW |
| 2708 | Standard EPROM, 1K × 8, 450 ns, light erasable | NOW |
| 2716 | Standard EPROM, 2K × 8, 450 ns, light erasable | NOW |
| 2111A-4 | Standard RAM, 256 × 4, 450 ns, common I/O | NOW |
| 2101A-4 | Standard RAM, 256 × 4, 450 ns, standard I/O | NOW |
| 5101 | Standard RAM, 256 × 4, 650 ns CMOS | NOW |
| 8255A | Programmable Peripheral Interface | NOW |
| 8251 | Programmable Communications Interface | NOW |
| 8214 | Priority Interrupt Controller | NOW |
| 8253 | Programmable Interval Timer | NOW |
| 8259 | Programmable Interrupt Controller | NOW |
| 8279 | Programmable Keyboard/Display Controller | NOW |

The 8748 is the best supported single chip microcomputer you can buy. To speed development there's the Intellec® Microcomputer Development System with assembly language programming, symbolic debugging, and full EPROM programming capability. The ICE-48™ In-Circuit Emulation module simplifies hardware/software integration and debugging. And the Intel Prompt-48™ Design Aid is a low cost, stand alone alternative for 8748 programming, simulation and debugging. Intel supports you from prototype to production with development software, documentation, training and application assistance.

The new 8748 will give manufacturers of instruments, terminals, communications equipment, controllers, electronic games, automotive products, home appliances and hundreds of other products the competitive edge. It will help you get better products to market ahead of the competition at lower cost.

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CIRCLE NUMBER 12

# Digital introduces DECstation. A big computer system that's small enough for anyone.

Digital put an amazing LSI version of the PDP-8 inside a DECscope, added some ingenious interconnecting devices and created something new. The DECstation. A complete computer system big enough to do all kinds of work and small, simple and inexpensive enough to do it for almost anyone.

**DECstation. A complete computer system in disguise.** It looks like a terminal, but look again. The DECstation has a powerful general purpose computer, a video terminal, a dual diskette drive, and its own special operating system. What's more, you can hook up two different printers and a second dual diskette drive. Then put the whole thing in a mini-desk, and when you're done you'll have the smallest big computer you've ever seen.

**The Video Data Processor. It's the big reason the DECstation's so small.** The VT78 Video Data Processor is a computer wrapped in a terminal. Inside the familiar DECscope you'll find an LSI version of the PDP-8 with 16K words (32K characters) of MOS memory and built-in interfaces. Two serial asynchronous ports feature speeds from 50 baud to 19.2 kilobaud. A disk port interfaces with up to 4 diskette drives. A parallel I/O port for printers and custom interfacing provides data transfer rates up to 180 kilobits/sec. All standard.

**You can go from carton to computer in less than an hour.** If you can push a button, you can run a DECstation. Because one button is all it takes to start things up. The bootstrap and self-test routines are built in.

Put it together, plug it in, and immediately you can begin to run anything from the PDP-8 software library. Which means you start with one of the most comprehensive sets of software tools available in a small system. Including two proven operating systems: OS/78 for stand alone applications and RTS/8 for real-time. OS/78, an extension of OS/8, supports a number of languages, including FORTRAN IV and BASIC. So all you have to do is load the operating system and start programming your application.

Whatever that application, if you're looking for a sophisticated little system, at the right price, and a remarkable OEM tool, consider DECstation. $7995 each. $5436 OEM quantity 50.

For our free brochure, write Digital Equipment Corporation, Parker Street, Maynard, MA 01754. European headquarters: 81 route de l'Aire, 1211 Geneva 26. Tel: 42 79 50. In Canada: Digital Equipment of Canada, Ltd.

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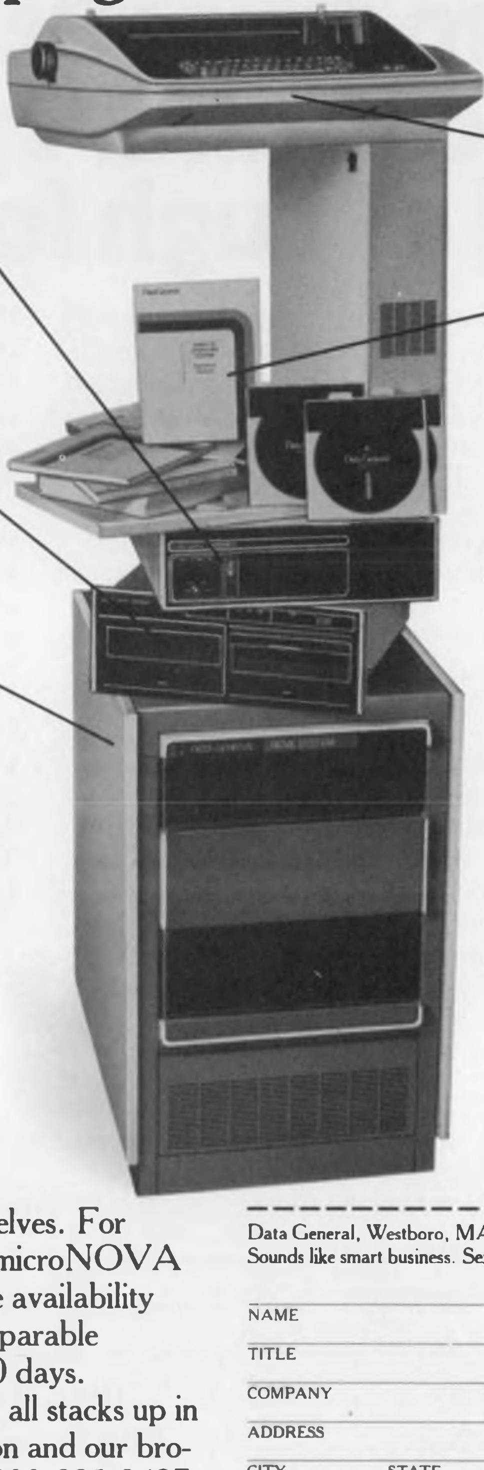
EC757

# Here's how Data General's microNOVA system stacks up against the competition.

**microNOVA Processor:**
Fully packaged 9-slot microcomputer, 16K words MOS memory, 2.4-microsecond arithmetic operations, hardware stack facility, multiply/divide, DMA capability. Includes RTC, PF/AR and APL. Supports up to 32K words RAM/PROM memory.

**Dual-diskette subsystem:**
Integral DMA controller, compact 630KB capacity.

**Cabinet:**
37 inches high, holds all rack mounted components.



**DASHER terminal printer:**
30 cps, 132-columns, typewriter keyboard, upper/lower case.

**Systems Software:**
Multitasking Disc Operating System, Real-Time Operating System, FORTRAN IV, Extended BASIC, Macro Assembler, Utilities.

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CIRCLE NUMBER 9

# Calculators lose keys, batteries—and gain timer

Two sources of trouble in handheld calculators—batteries and keys—are eliminated in new liquid-crystal-display units unveiled at the recent Consumer Electronics Show. Other units, featured by at least four manufacturers in Chicago, combine a calculator and a calendar-watch and timer in the same LCD unit.

Neither batteries nor an on-off switch are needed by a solar-cell-powered calculator, the Photon, by Teal Industries, Carson, CA (see photo). The Photon should not be confused with battery-operated calculators having solar-cell battery chargers (see ED 5, Mar. 1, 1977, p. 26). Rather, it operates continuously in ambient light levels ranging from daylight to candlelight. The solar cells, produced by Solarex, Rockville, MD, are designed for maximum efficiency at low-light levels.

Eleven calculator functions are provided, including full direct-access memory. The solar cell has a five-year warranty. List price is $99.95.

An eight-digit LCD calculator, called the Super Thin Man, also has no keys—or any other moving part. Instead of keys, the unit by Sharp Electronics, Paramus, NJ, has a flat, touch-sensitive electronic control panel.

The panel's data-entry locations are solid and flush with the surface of the 3/16th-in.-thick unit, so they don't provide the usual key-entry "feel." Instead, audio input is verified by a beeper, which emits a pleasant chirp each time a key spot is touched. The beeper can also be turned off.

In addition to standard math functions, square root, per cent, and a four-key, independently addressable memory are provided by the Sharp unit. In the beeper mode, the calculator operates about 400 hours on two silver-oxide cells. In the silent mode, operation can be extended to 600 hours.

An automatic power-off feature shuts the unit down a few moments after calculators are completed. Suggested price is $34.95.

Meanwhile, a new trend has emerged—combining LCD calculators and clock-timers in small, hand-held units. For example, the TimeCalc by Royal Typewriter of Hartford, CT, is a wallet-type device with two independent LCD displays—an 8-digit for the calculator and a 4-digit hours-and-minutes display for the clock. The latter, which is on continuously, also has AM and PM indicators and a night-light. Two keys are used to set the clock.

The calculator is a standard four-function unit with square root, percentage and memory keys. When the memory is being used, an indicator appears in the calculator display.

Suggested price is $59.95, and the unit is estimated to operate for one year on three silver-oxide cells.

A combination unit by Sharp—the CT500—has a single display either for eight digits for the standard calculator output or for six digits (hours, minutes and seconds) of the crystal-controlled clock. The clock has a beeper alarm as well as a calendar featuring the date, month, year and week. The time at key cities throughout the world can be displayed, on a 12 or 24-hour basis. Stopwatch circuits permit a count-up or count-down, which can be initiated by pressing certain keys. It sells for $79.95.

A crystal-controlled timepiece, stopwatch, timer and calculator are combined in Casio's MQ-1 personal palm-sized unit. Its LCD display has six digits, but the internal computing capacity and time calculations are useful up to eight digits.

The calendar is programmed for days, months of all lengths, and leap years from 1901 to 2099. The stopwatch can cover 23 hours, 59 minutes and 59.5 seconds before reverting to zero. Price is $59.95

**Solar-cell powered calculator** from Teal Industries operates at low light levels.

**Sharp's CT500 calculator** can display the time in key world cities.

## Lowest-cost 16-bit mini leads computer-kit line

A 16-bit minicomputer that is half the price of current comparable 16-bit minis tops a line of computer kits from Heath Co., Benton Harbor, MI. An 8-bit mini, a video terminal, and a paper-tape reader/punch have also been introduced.

The 16-bit H11, $1295 in its basic form, incorporates an LSI-11 single-board computer from Digital Equipment Corp. of Maynard, MA. The board has been wired and tested.

Even with options such as additional memory and interface circuitry that make the H11 equivalent to a DEC PDP-11/03, the H11's price—near $2500—is half that of the DEC machine. Among the optional boards available from Heath are the H11-1 4-k memory, $275, the H11-2 parallel interface, $95, and the H11-5 serial interface, $95.

DEC will provide service and some software support on the CPU board. Heath will provide service and support for the rest of the H11 and for the other equipment in the line. Purchasers of the H11 will be eligible to join the Digital Equipment Computer Users Society and take advantage of the DECUS software library.

Included in the base price of the H11 kit is a software package that includes assembly and high-level languages such as Focal and Basic.

Basic-language software—as well as editor and assembler programs—is also included with the H8, an 8-bit mini based on an 8080-type microprocessor. The $375 H8's front panel has a 9-digit octal display and keyboard for simple programming and for reading out register and memory contents while programs are running.

Unlike other low-cost computers aimed at the hobby and small-business markets, the H8 does not use the 100-pin standard bus developed by MITS Inc., Albuquerque, NM. The H8's bus is built on a 10-slot motherboard containing 50-pin connectors. The MITS Altair S-100 bus is too expensive and has some technical problems such as overly critical timing, says Lou Frenzel, Heath's director of educational and computer product development.

The video terminal kit in the Heath line, the H9 CRT terminal kit, $530, has a 67-key keyboard and displays uppercase characters in 12 lines of 80 characters on a 12-in screen. Cursor control, a batch-transmit mode, and limited plotting facilities are featured on the terminal.

For permanent program storage, the $350 H10 paper tape reader/punch uses standard 1-in. roll or fan-fold 8-level paper tape. The reader section operates at 50 characters/s, and the punch operates at 10 characters/s.

In addition to its own computers and peripherals, Heath is marketing a 30-cps teleprinter, the LA36 DEC writer II. While the price hasn't been set, it will be close to the $1800 price charged by other DEC sales outlets.

**CIRCLE NO. 318**

## TI's new op amps use much less power

The latest operational amplifiers to combine bipolar and field-effect transistors consume an order of magnitude less power, or less than half the input noise, of their general-purpose predecessors.

Introduced this week by Texas Instruments Inc., Dallas, the new op amps complement the firm's TL080 series of Bifet devices, and are divided into the low-power TL060 family and the low-noise TL070 family.

With no load and no signal, a TL060 device consumes about 0.1 mA of power-supply current, compared to 2.8 mA for a similar TL080 device. Equivalent input noise voltage of a TL070 op amp is only 20 nV $\sqrt{Hz}$, less than half the 47 nV $\sqrt{Hz}$ for a comparable TL080 series circuit.

The low-power versions are aimed at multiple op amp applications such as active filter and modems. The low-noise devices are designed to be used in audio amplifiers.

A commercial op amp in an 8-pin plastic DIP is priced at about $.50

**CIRCLE NO. 319**

## Perform calculations or tell time—on the phone

Add an eight-digit calculator and an electronic calendar-clock to a pushbutton telephone and what do you get? The Figure-Phone, with a 20-button keyboard and a LED display that can give the time, show any number dialed, or present calculated results. It also permits you to perform calculations while talking on the phone.

The Figure-Phone calculator, which is selected by pressing a CAL key, has standard arithmetic functions plus percent. You select the clock function with another key. The clock shows hours and minutes in the LED display and also lights a separate AM or PM LED indicator. An audible alarm is built into the system so the clock can be used as a timer.

The calendar features of the Figure-Phone—developed by Circuit Service of Des Plaines, IL for Phone Devices Corp., Chicago—can display the day, month and year with an automatic update for 100 years. The clock's time base is derived from the 50 or 60-cycle ac line powering the phone circuits.

Lifting the receiver off the hook automatically sets the system in the dialing mode. The phone number keyed in appears in the LED display.

When the call is answered, you can select the calculator function or the time display. The last number dialed is held in memory and can be redialed by pressing a special key.

The orignal version of the phone used a calculator and a clock chip from Texas Instruments, but the new units have a single dedicated chip from TI that combines all functions.

The single-line Figure-Phone for pushbutton phone systems cost $219.50, while the one for a rotary dial system if $269.50, due to added interface components.

## First development system for bit-slice μPs

The first development system for bit-slice microprocessors will be introduced this fall. A prototyping tool similar in concept to the available development systems for fixed-instruction-set MOS microprocessors, the System 29 from Advanced Micro Devices, Sunnyvale, CA, is a general-purpose design. It supports the prototyping, microcoding and programming of any microprogram system—regardless of its architecture—and works with any bit slices—the Intel 3000 and the National IMP as well as the AMD 2901 bipolar family.

Hardware debugging and microcode assembly/debugging are computer-assisted. The AMD 9080A microprocessor included in System 29 is supported by the AMDOS/29 disc-operating system and the AMDASM/29 microcode assembler, which reside on dual floppys.

Composed of a "breadbox" logic card enclosure, a CRT/keyboard terminal, and a disc package, the bench-top system includes universal boards on which the prototype system may be assembled, the main control processor with 32 kbytes of memory, and a RAM microprogram memory of up to 4 k × 128 bits.

"Since each bit-slice design is different, costly prototyping and microcode-development tools have been built up each time, but little of the work expended on one design is transferable to the next," says John Springer, AMD's bipolar marketing manager. "The designer can avoid these high repeat costs with System 29, and he can build his prototypes either inside the System 29 breadbox on our universal card or externally by using available interfaces and cables that plug into PROM sockets on his own PC boards."

# A resistor for all reasons

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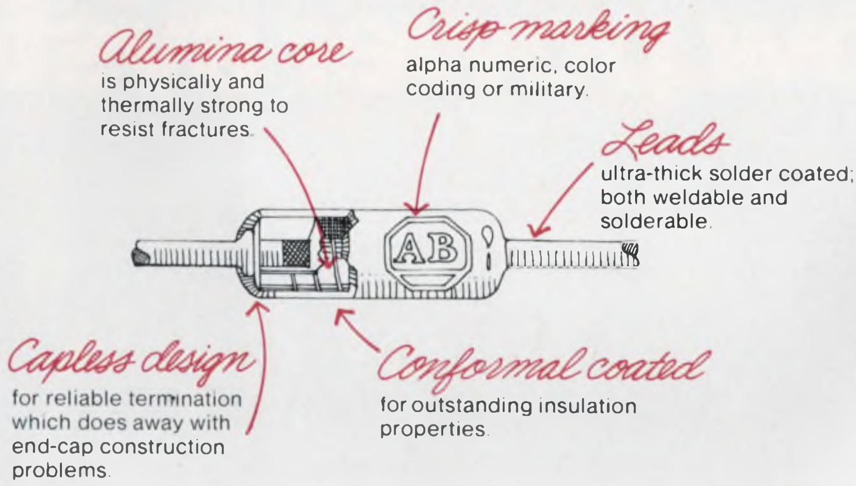


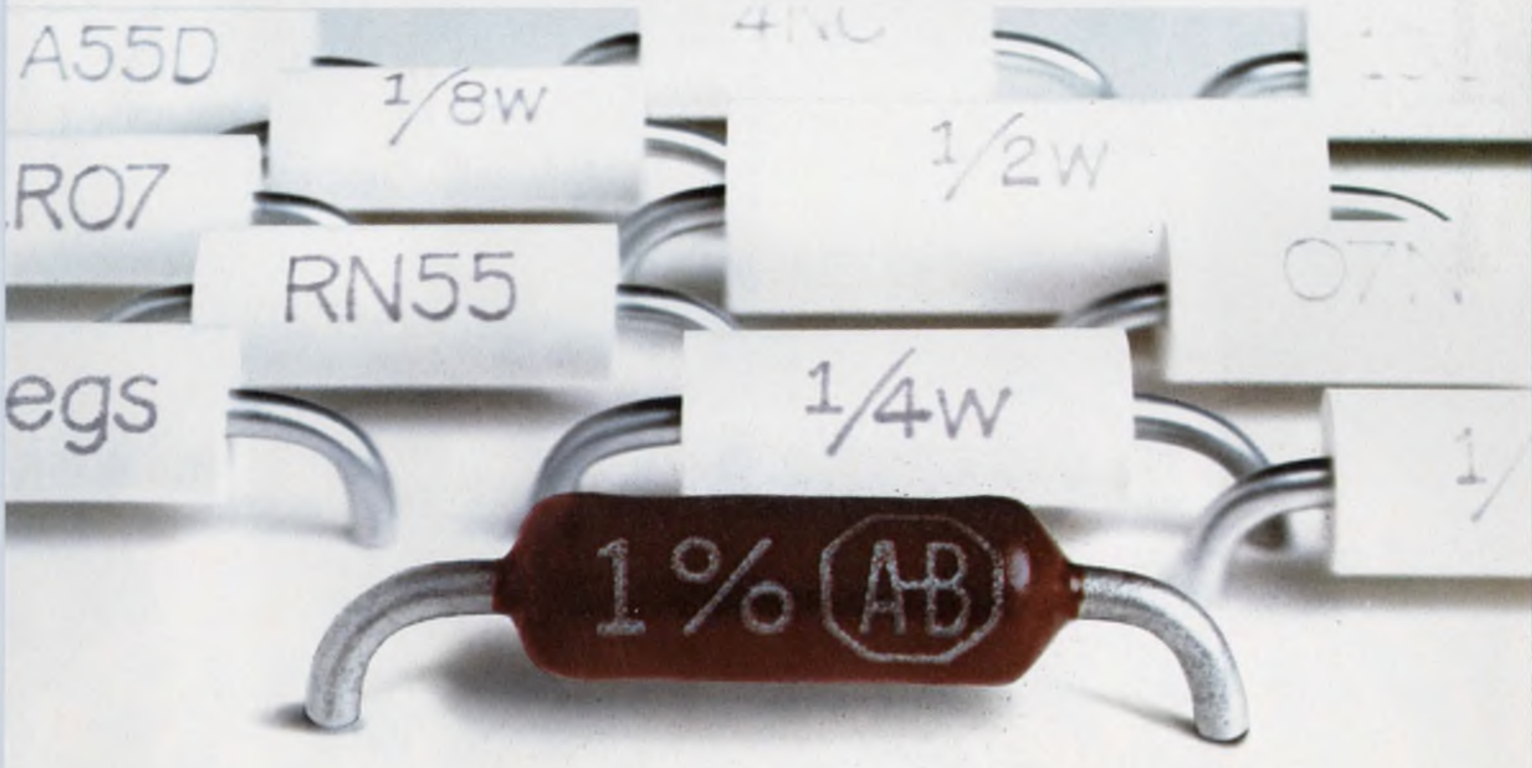


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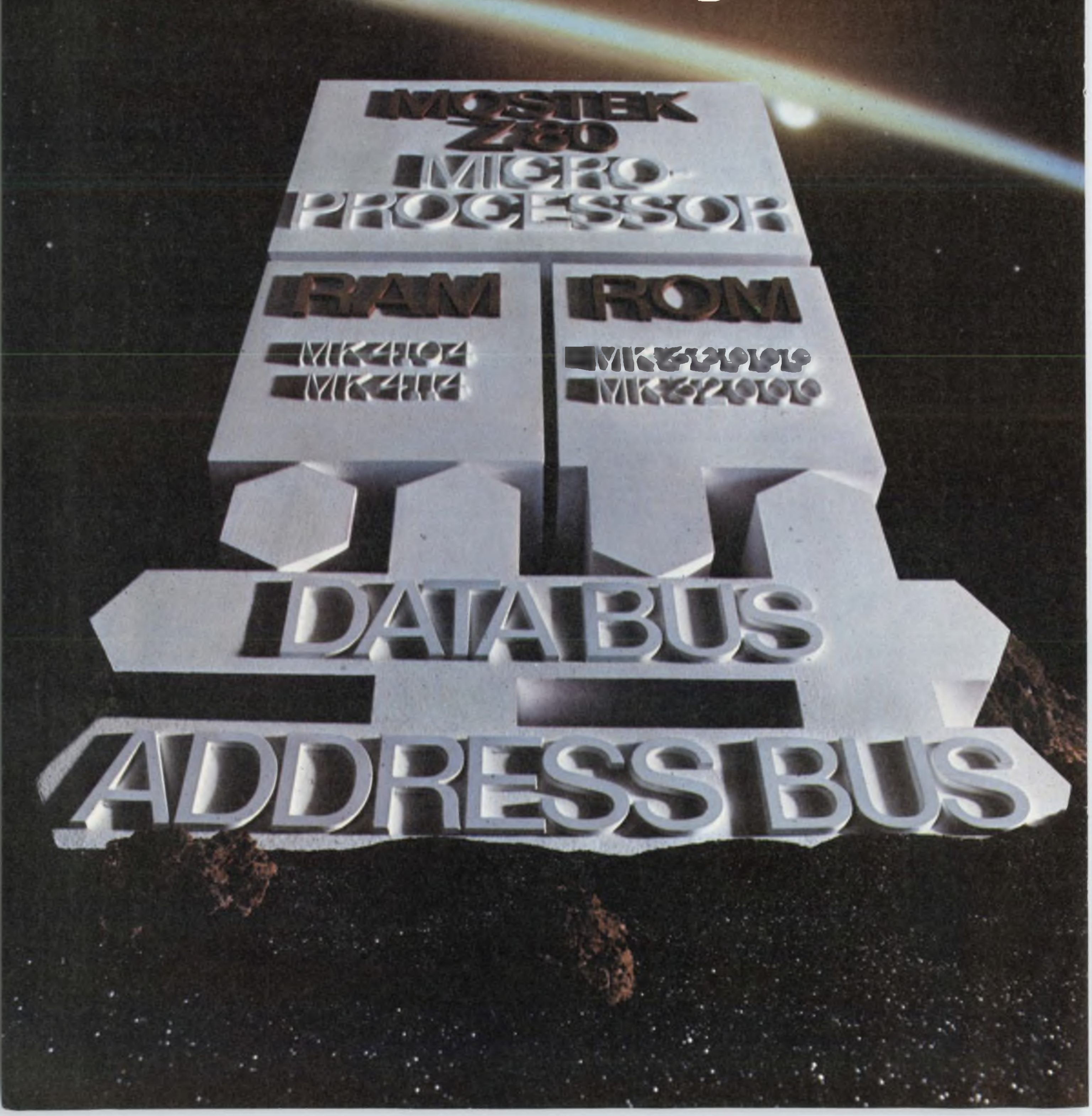
CIRCLE NUMBER 13

# Mostek takes you forward to a new era in low power systems.



# Introducing the Edge-Activated™ Series.

Higher density, lower power and simplified system design. That's the idea behind Mostek's Edge-Activated Series. The series includes a complete family of high-density static RAMs and ROMs, with a wide selection of organizations. All devices are implemented with the same edge-activated circuit design concept which allows you to design a +5V only system without compromising speed or power. It's the best of both worlds.

**Proven design techniques for maximum performance.**

Mostek's approach integrates a static MOS storage cell with dynamic MOS periphery so that the full advantages of the technology can be realized. Now your applications can be implemented with a minimum number of devices. Also, edge-activated devices operate at faster speeds than traditional static circuits but with much lower power dissipation.

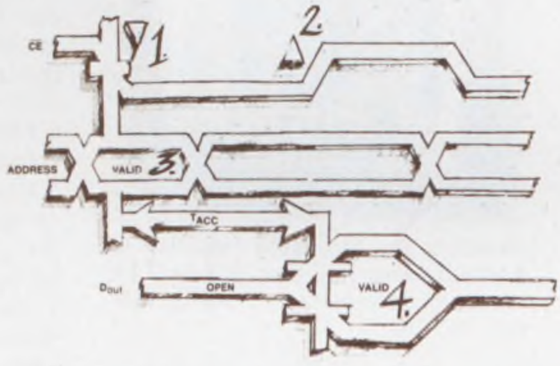
Other system benefits include . . .

- totally static operation—no refresh required
- single +5V power supply—±10% tolerance
- on-chip address latches
- active and standby power—lowest in the industry
- reduced $V_{CC}$ for battery back-up applications
- direct TTL compatibility and common I/O operation

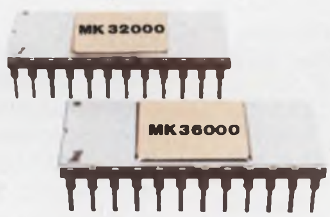
**Let's put a dollar value on lower power.**

One common timing signal, provided in almost every memory application, activates the entire family of devices. However, if the clock signal must be provided externally, the system benefits of lower power far outweigh design complexity. An example is a 16K × 9-bit storage matrix. Designed with edge-activated MK 4104's, this system would dissipate less than 1 watt in the memory array, while the same system with static-interface RAMs would dissipate approximately 18 watts. Since typical power sub-system designs cost from $1.00 to $1.50 per watt, both design and cooling costs are reduced significantly.

Data Sheets, Application Notes, price and delivery are available from Mostek field sales representatives.




*A simple high to low transistion at the Chip Enable input (1) activates the entire family of memory devices. Returning the CE input to a high level (2) achieves a 75% reduction in device operating power for an automatic standby power mode. Address information is strobed and latched (3) into a set of on-chip registers, thereby eliminating "set up" time requirements and minimizing "hold" time. While data is valid (4) you have full control of the Data Output.*





**The Edge-Activated™ Series**

| | Access Time (max) | Active Power (max) | Standby Power | Industry Standard Pin Configuration |
|---|---|---|---|---|
| MK4104 (4K×1 RAM) | 200 ns | 120 mW | 30 mW | 18 pin |
| MK4114 (1K×4 RAM) | 200 ns | 120 mW | 30 mW | 18 pin |
| MK32000 (4K×8 ROM) | 300 ns | 200 mW | 25 mW | 24 pin |
| MK36000 (8K×8 ROM) | 300 ns | 200 mW | 25 mW | 24 pin |

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CIRCLE NUMBER 11

# Choosing a $\mu$P by its capabilities is a growing 'family affair'

Now that there are over 50 different processors to choose from, the designer often can find exactly what he needs in a standard product. Choosing begins with three basic processor families:

- The all-in-one, which has the RAM, ROM, clock and I/O on the chip.
- The general-purpose, which requires external ROM, RAM, clock and I/O circuits.
- The bit-slice, which is made from cascadable logic sections and also requires external RAM, ROM and I/O circuits.

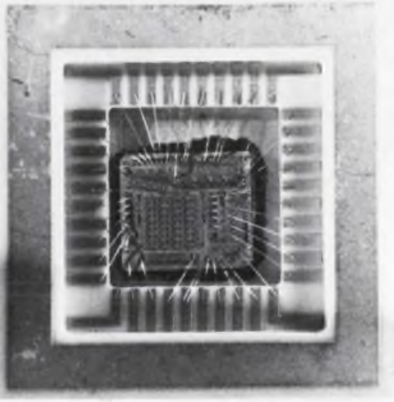
Of course, there's much more to finding the best $\mu$P than picking a family. (For a summary of many of the various $\mu$P specifications, see Tables 1, 2 and 3). All-in-one processors, for example, offer low-cost solutions to many control applications. They aren't new—Rockwell and Texas Instruments have been selling 4-bit units for several years. What *is* new, though, is the advent of 8-bit all-in-one microcomputers on a chip.

### One-chip computer fits the bill

Currently, only a few 8-bit one-chips are available—the PIC-1650 from General Instrument, the 8048/8748 from Intel and the 3870 from Mostek. But there will be nearly twice as many by the end of this year. A dedicated controller, the 6400, and a trimmed version of the 6800 processor, the 6801, will come from Motorola while Zilog will offer the Z8, an all-in-one version of the Z80. Many of the performance specs of the unavailable circuits are yet to be set, but the Z8 reportedly has a 96 × 8 RAM and a 2048 × 8 ROM. Its instructions will be a subset of the Z80 command set. Details of the Motorola

**Dave Bursky**
Associate Editor

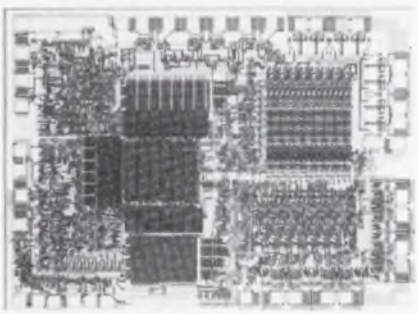
**Dave Barnes**
Western Editor



**Boasting the strongest following of alternate sources,** the 2901 ALU bit slice was developed by Advanced Micro Devices.

chips are even skimpier, but the 6400 is said to have a 32 × 8 RAM and a 1024 × 8 ROM. Also coming is the Micromachine from Fairchild, a chip very similar to Mostek's 3870. And Intel will soon announce a 2 k × 8 version of its 8048 all-in-one processor.

The four available 8-bit chips have ROM capacities ranging from 512 × 12 for the PIC-1650 to 2048 × 8 for the 3870. The PIC-1650 has a 32-byte RAM, but the other units have 64-byte RAMs. General Instrument, though, is planning some design tradeoffs on the 1650 processor—larger ROM versions and fewer I/O-line models. Also on the way is a version that has a real-time clock and a power-down capability that



**Bus control logic and a clock** as well as two instructions are added to the 8080A by Intel to make the 8085.

maintains the real-time clock. $I^2L$ will probably be used for the power-down model since it can operate on a 1-V supply, according to Frank Jelenko, a GI product engineering manager.

The field of 4-bit all-in-one processors offers a choice of more than 20 models from about a half-dozen manufacturers. The latest company to join the fray, NEC Microcomputers, offers a PMOS-chip series—the $\mu$PD 545, 6, 7 and 8.

Most of the NEC chips are intended for specific applications. For instance, the $\mu$PD 548 is designed to handle keyboards. The 547 is similar, but has a smaller ROM and instruction set—the 546 is more of a controller since it has a 6-bit programmable timer. The 545 is designed for driving high-voltage displays, which are commonly used in electronic cash registers.

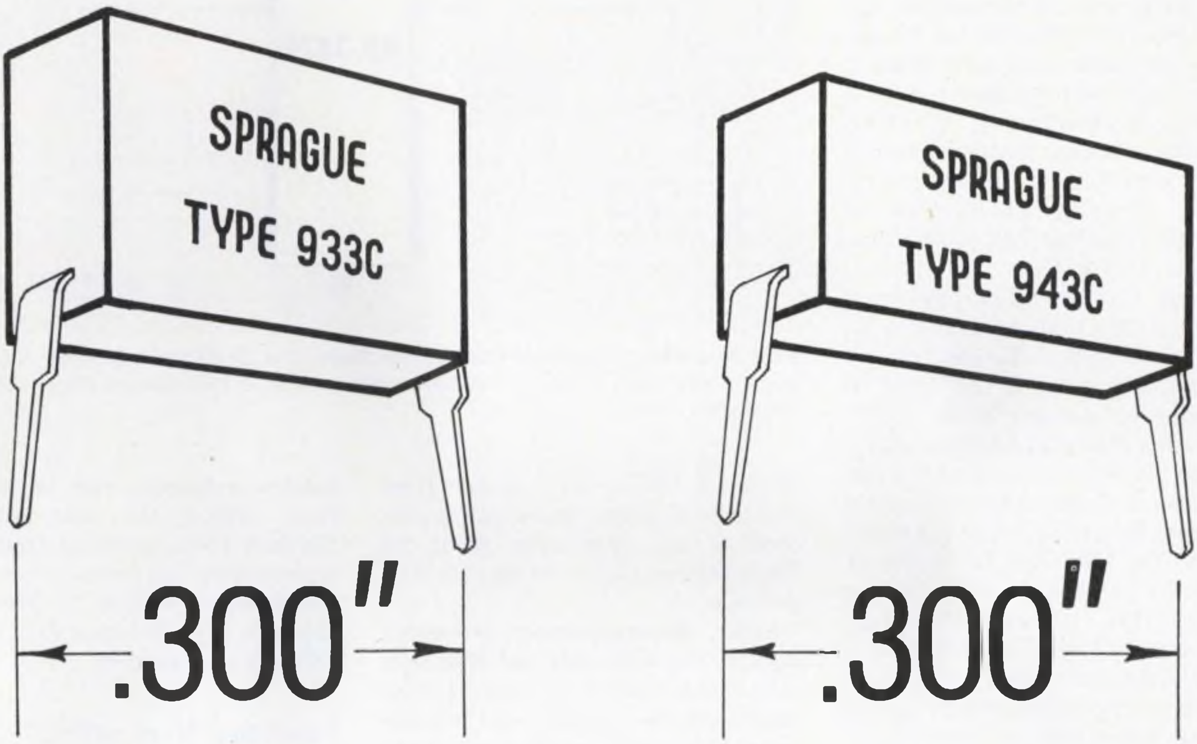
### Other firms, similar products

Rockwell's line of one-chip microcomputers is also expanding from its MM76, 77 and 78 products, which include RAMs of 48, 96 and 128 × 4, respectively. On-board ROMs range from 640 × 8 to 2048 × 8. Newer chips in the series include the MM76/C, 76/D, 76/E and 76/L, as well as the MM75. The C version is similar to the MM76 except that a high-speed counter is fabricated on the chip, which comes in a 52-pin DIP instead of a 42-pin package. Unavailable until the end of the year, the D version will include an analog-to-digital converter on the processor chip and also come in a 52-pin package.

The E version is the MM76 with a larger memory capacity, while the L version operates at lower voltages and comes in a standard 40-pin DIP. The MM75, which offers only 22 I/O lines, can be used for smaller I/O applications. Moreover, it comes in an inexpensive 28-pin DIP.

Two major series of processors from

# COMPATIBILITY!

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CIRCLE NUMBER 20

Texas Instruments are also undergoing some sprucing up. The TMS-1000 and TMS-1100 series of PMOS processors are now available in higher-speed NMOS versions as well as in high-voltage models to handle up to 35 V. Since both the TMS-1000 and 1100 series parts are pin-compatible, upgrades from the TMS-1000 are simple.

Only one other company offers a family of all-in-one processor chips—National Semiconductor. Its COPS (calculator-oriented processor-series) family consists of three general purpose one-chip processors—the MM57140, 57152 and 5799—and a two-chip set, the 5781/82.

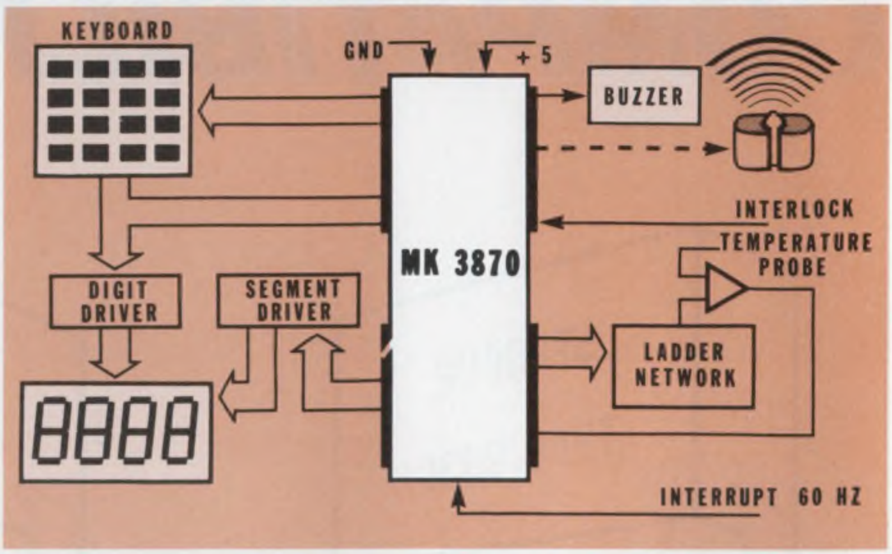
Besides the general-purpose computer on a chip, preprogrammed solutions are being offered for some control problems. For instance, the MM57109 (a specialized member of the COPS family) is a dedicated scientific-calculator circuit that can be added to a bus to take some of the burden off a main processor. Two other preprogrammed circuits—the TMS-1018 (a version of the TMS-1000) and the TMS-1117 (a version of the 1100)—are offered by Texas Instruments. The former is a dedicated number cruncher; the latter is a controller programmed to handle microwave-oven control inputs.

### Multiple-chip sets also do the job

Some of the not-so-new all-in-one processors aren't single-chip but two or three-chip sets—such as the PPS-4, PPS-4/2, PPS-8 and PPS-8/2 from Rockwell. Although these circuits are selling well, many designers are looking to the newer one-chip processors for new designs.

In some applications, even a 4-bit processor may be overkill in terms of the processing power needed. To eliminate some of the cost and excess power, General Instrument has developed a Sequential Boolean Analyzer. This processor is a 1-bit system with a 128 × 1 internal RAM, a 1024 × 8 program ROM and 31 I/O lines—all in a 40-pin DIP. It has just eight basic instructions and can cycle through its entire program without interrupts. In production quantities, a simple controller like this is expected to cost about $1.

General-purpose processors haven't faded away. The smallest, but newest addition to the rolls is a 1-bit general-purpose processor produced by Motorola—the CMOS MC14500B. It requires an external program counter, external memory and I/O support circuits, but since it is CMOS, it can operate from a 3 to 18-V supply and requires only about 1 mA. (For more about the MC14500B see ED No. 10, May 10, 1977, p. 106.)




**Able to perform multiple control functions,** the 3870 from Mostek is software compatible with the F-8 and can easily act as a microwave oven controller, as shown here.

Older, general-purpose processors such as the 4-bit 4004 and 4040 have just about reached the end of their design-in cycle—the all-in-one processors put all their processing power and more on a single chip. However, one general-purpose newcomer to the 4-bit market, NEC Microcomputers' μPD 541, has 69 basic instructions, a 4096-word addressing range and keyboard and display interfacing.

All other general-purpose microprocessors have 8-bit data word lengths or longer—from the old 8008 from Intel to the most exotic $I^2L$ SBP9900 16-bit processor from Texas Instruments. The newest processors in this grouping include the 8085 from Intel, the CDP1803 from RCA and the 8X300 from Signetics.

### Expanding from within

Meanwhile, some of the general-purpose processor lines introduced a year or two ago are starting to expand. Two 8-bit devices, for example, are planned by Motorola for 1978.

One of them, tentatively dubbed the 6809, will have an enhanced 6800 instruction set and an on-chip clock. The

## μPs: only part of the whole

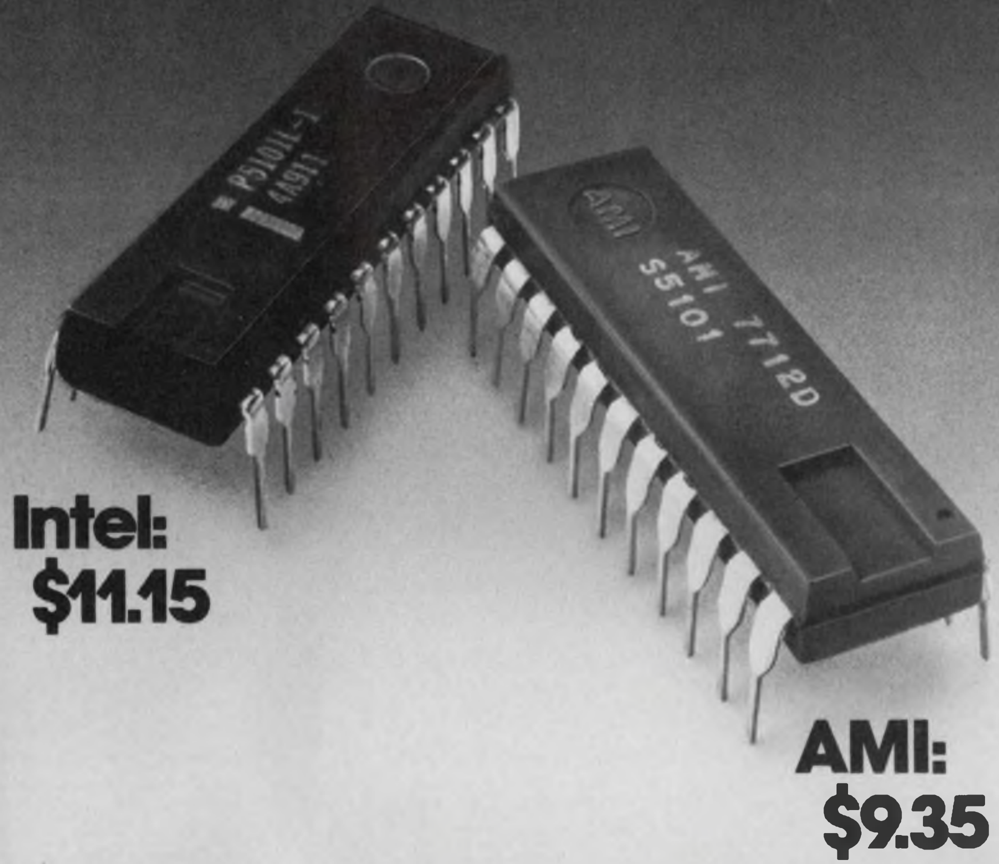
Along with improvements in microprocessor chips has come a shift toward treating the devices as part of a system, rather than as isolated components. A great deal of processing power can be added—and much software and memory cost saved—by using the I/O controllers, direct-memory-access chips, high-speed arithmetic units and other "helpers" available in the form of peripheral chips (see ED 10, May 10, 1977, p. 32).

"Semiconductor manufacturers and users are realizing that the CPU is a small part of the cost," says Al Weissberger, senior staff engineer at Signetics Corp. in Sunnyvale, CA. "The more expensive part is the I/O circuitry."

As a result, today's alert designer is less likely to pick a CPU and go on from there, but more likely to compare several total systems solutions that include the μP, and the support devices, and the software.

He may even be able to take advantage of a mix of elements from different suppliers.

"There will be a lot of mixing of chips," says Ben Anexter, MOS marketing manager for Advanced Micro Devices of Sunnyvale. "One-stop shopping is on its way out. Instead, designers will choose the best individual parts from the product lines of different companies." Some firms, in fact, like Standard Microsystems Corp. of Hauppauge, NY, specialize in system support chips and don't make microprocessor CPUs at all.

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CIRCLE NUMBER 21

# Table 1. Microprocessors in brief

| Manufacturer | Processor | Process technology | Word size (data/instruction) | Direct addressing range (words) | Number of basic instructions | Maximum clock frequency (MHz)/phases | Instructin time shortest/longest[2] (μs) | TTL compatible | BCD arithmetic | On-chip interrupts/levels | Number of internal general-purpose registers | Number of stack registers | On-chip clock | DMA capability | Specialized Memory & I/O circuits avail. | Prototyping system avail. | Package size (pins) | Voltages required (V) | Assembly language development system | High-level languages | Time-sharing cross software | Comments | Circle number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Motorola | MC14500 | CMOS | 1/4 | 0 | 16 | 1/1 | 1/1 | Yes | No | Yes/1 | 1 | 0 | Yes | No | No[4] | No | 16 | 3 to 18 | No | No | No | Needs external program counter | 451 |
| Intel | 4004 | PMOS | 4/8 | 4k | 46 | 0.74/2 | 10.8/21.6 | No | Yes | Yes/1 | 16 | 3x12 | No | No | Yes | No | 16 | 15 | Yes | Yes | Yes | Superseded by 4040 | 452 |
| Intel | 4040 | PMOS | 4/8 | 8k | 60 | 0.74/2 | 10.8/21.6 | No | Yes | Yes/1 | 24 | 7x12 | No | No | Yes | Yes | 24 | 15 | Yes | Yes | Yes | General-purpose 4-bit μP | 453 |
| NEC Microcomputers | μPD541 | PMOS | 4/8 | 4k | 69 | 0.5/2 | 6.4/38.4 | Yes | Yes | Yes/8 | 4 | 8x12 | No | Yes | Yes | Yes | 42 | 5, −5 | Yes | No | No | Intended for electronic cash registers, etc. | 454 |
| Fairchild | 2 chip F8 | NMOS | 8/8 | 64k | 69 | 2/1 | 2/13 | Yes | Yes | Yes/1 | 64 | RAM | Yes | Yes | Yes | Yes | 40 | 5,12 | Yes | Yes | Yes | Usually used with program storage unit | 455 |
| Ferranti F100L | | | | | | | | | | | | | | | | | | | | | | | 456 |
| General Instrument | 8000 | PMOS | 8/8 | 1k | 48 | 0.8/2 | 1.25/3.75 | No | Yes | Yes/1 | 48 | 0 | No | No | Yes | Yes | 40 | 5, −12 | No | Yes | Yes | Predecessor of F8 | 457 |
| Intel | 8008 | NMOS | 8/8 | 16k | 48 | 0.8/2 | 12.5/37.5 | No | Yes | Yes/1 | 6 | 7x14 | No | No | Yes | Yes | 18 | 5, −9 | Yes | Yes | Yes | Predecessor of 8080, still in wide use | 458 |
| Intel | 8080A | NMOS | 8/8 | 64k | 78 | 2.6/2 | 1.5/3.75 | Yes[3] | Yes | Yes/1 | 8 | RAM | No | Yes | Yes | Yes | 40 | 5,12, −5 | Yes | Yes | Yes | By and large, still the most popular | 459 |
| Intel | 8085 | NMOS | 8/8 | 64k | 80 | 3/1 | 1.3/5.85 | Yes | Yes | Yes/4 | 8 | RAM | Yes | Yes | Yes | Yes | 40 | 5 | Yes | Yes | Yes | 8080 code compatible, has built-in clock | 460 |
| MOS Technology | MCS-650X | NMOS | 8/8 | 64k | 56 | 4/1 | 0.5/3.5 | Yes | Yes | Yes/1 | 0 | RAM | Yes | No | Yes | Yes | 40 | 5 | Yes | Yes | Yes | Provides 13 addressing modes | 461 |
| MOS Technology | MCS-651X | NMOS | 8/8 | 64k | 56 | 4/2 | 0.5/3.5 | Yes | Yes | Yes/1 | 0 | RAM | No | No | Yes | Yes | 40 | 5 | Yes | Yes | Yes | Similar to 650X but needs 2Φ clock | 462 |
| Motorola | M6800 | NMOS | 8/8 | 64k | 89 | 2/1 | 1/2.5 | Yes | Yes | Yes/1 | 0 | RAM | No | Yes | Yes | Yes | 40 | 5 | Yes | Yes | Yes | Available in new depletion-load version | 463 |
| Motorola | M6809 | NMOS | 8/8 | 64k | 100+ | 2/1 | 2/5 | Yes | Yes | Yes/1 | 0 | RAM | Yes | Yes | Yes | Yes | 40 | 5 | Yes | Yes | Yes | Enhanced 6800 command set | 464 |
| Motorola | M6802 | NMOS | 8/8 | 64k | 89 | 2/1 | 2/5 | Yes | Yes | Yes/1 | 0 | RAM | Yes | Yes | Yes | Yes | 40 | 5 | Yes | Yes | Yes | Has 128 x 8 on-chip RAM | 465 |
| National Semiconductor | SC/MP | PMOS NMOS | 8/8 | 64k | 46 | 4/1 | 5/10 | NMOS only | Yes | Yes/1 | 0 | RAM | Yes | Yes | No[4] | Yes | 40 | 5, −7 | Yes | Yes | Yes | Has handy daisy-chain capability | 466 |
| NEC Microcomputers | μPD 8080A | NMOS | 8/8 | 64k | 78 | 2/2 | 1.92/8.16 | Yes[3] | Yes | Yes/1 | 8 | RAM | No | Yes | Yes | Yes | 40 | 5,12, −5 | Yes | Yes | Yes | Pin compatible but does BCD subtraction | 467 |
| RCA | 1802 | CMOS | 8/8 | 64k | 91 | 6.4/1 | 2.5/3.75 | Yes | Yes | Yes/1 | 16 | RAM | Yes | Yes | Yes | Yes | 40 | 3 to 12 | Yes | Yes | Yes | Superseded two-chip version | 468 |
| RCA | 1803 | CMOS | 8/8 | 64k | 91 | 6.4/1 | 2.5/3.75 | Yes | Yes | Yes/1 | 16 | RAM | Yes | Yes | Yes | Yes | 28 | 3 to 12 | Yes | Yes | Yes | Trimmed down version of 1802 | 469 |
| Scientific Microsystems | SMS-300 | Bip | 8/8 | 8k+ | 8 | 10/1 | | Yes | No | No | | 0 | No | | Yes | | 50 | | No | Yes | Yes | Very specialized instruction set | 470 |
| Signetics | 2650 | NMOS | 8/8 | 32k | 75 | 1.2/1 | 4.8/9.6 | Yes | Yes | Yes/1 | 7 | 8x15 | No | Yes | Yes | Yes | 40 | 5 | Yes | Yes | Yes | Has two higher speed versions | 471 |
| Zilog | Z80 | NMOS | 8/8 | 64k | 150+ | 4/1 | 1/5.75 | Yes | Yes | Yes/1 | 14 | RAM | No | Yes | Yes | Yes | 40 | 5 | Yes | Yes | Yes | 8080 instructions are a subset | 472 |
| Intersil | 6100 | CMOS | 12/12 | 4k | 81 | 4/1 | 2.5/5.5 | Yes | No | Yes/1 | 0 | RAM | Yes | Yes | Yes | Yes | 40 | 4 to 11 | Yes | Yes | Yes | Emulates PDP-8 instruction set | 473 |
| Toshiba | T3190 | PMOS NMOS | 12/12 | 4k | 108 | 2.5/1 | 10/30 | Yes | No | Yes/8 | 8 | RAM | Yes | Yes | Yes | Yes | 36 | 5, −5 | Yes | Yes | Yes | Has multiply and divide inst. | 474 |
| Data General | Mn601 | NMOS | 16/16 | 32k | 42 | 8.33/2 | 1.2/29.5 | Yes | No | Yes/1 | 4 | RAM | Yes | Yes | Yes | No | 40 | 5,10,14, −4.25 | Yes | Yes | Yes | Emulates NOVA instruction set | 475 |
| Fairchild | 9440 | I²L | 16/16 | 64k | 42 | 10/1 | | Yes | No | Yes/1 | 4 | RAM | Yes | Yes | No[4] | No | 40 | | No | No | No | Emulates NOVA instruction set | 476 |
| General Instument | CP1600 | NMOS | 16/16 | 64k | 87 | 4/2 | 1.6/4.8 | Yes | No | Yes/1 | 8 | RAM | No | Yes | Yes | Yes | 40 | 5,12, −3 | Yes | Yes | Yes | All internal registers can be accumulators | 477 |
| National Semiconductor | PACE | PMOS | 16/16 | 64k | 45 | 2/2 | 2.5/5 | No | Yes | Yes/6 | 4 | 10x16 | No | Yes | Yes | Yes | 40 | 5,8, −12 | Yes | Yes | Yes | Architecture intended for data handling | 478 |
| Panafacom | L-16A | NMOS | 16/16 | 64k | 33 | 2/2 | 2/6 | Yes[3] | No | Yes/3 | 5 | RAM | No | Yes | Yes | No | 40 | 5,12, −3 | Yes | No | No | | 479 |
| Texas Instruments | TMS9980 | NMOS | 16/16[1] | 16k | 69 | 4/4 | 3.2/49.6 | Yes[3] | No | Yes/4 | 16 | RAM | Yes | Yes | Yes | No | 40 | 5,12, −5 | Yes | Yes | Yes | Small version of TMS 9900 | 480 |
| Texas Instruments | TMS9900 | NMOS I²L | 16/16 | 64k | 69 | 4/4 | 2/31 | Yes[3] | No | Yes/16 | 16 | RAM | No | Yes | Yes | No | 64 | 5,12, −5 | Yes | Yes | Yes | Emulates 990 mini instructions | 481 |

1. Has 8-bit external buses and 16-bit internal buses 2. With maximum clock 3. Except clock lines 4. Standard TTL or MOS circuits will suffice

*(continued on page 32)*

# Table 2. All-in-one processors

| Company | Device | Process technology | Word size in bits (data/inst.) | On-chip RAM size (words) | On-chip ROM/PROM size (words) | Off-chip memory expansion | Number of basic instructions | Maximum clock frequency (kHz) | On-chip clock | Instruction time (shortest/longest) μs | TTL compatible | BCD arithmetic | On-chip interrupts/levels | Subroutine nesting levels | General-purpose internal registers | Number of I/O lines | Additional special support circuits | Package size (DIP pins) | Voltages required (V) | Prototyping system avail. | Assembly language programming system | High-level language programming system | Time-sharing cross software | Comments | Circle number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| General Instrument | SBA | NMOS | 1/8 | 120×1 | 1024×8 | No | 8 | 800 | Yes | 1.25/1.25 | Yes | No | No | 16 | RAM | 31 | No | 40 | 5,12 | Yes | No | No | No | Will have expandable version | 482 |
| Essex International | SX-200 | PMOS | 4/8 | 64×4 | 1024×8 | Yes | 41 | 400 | Yes | 20/20 | No | Yes | Yes/1 | 1 | RAM | 16 | No | 28 | 10 to 20 | Yes | Yes | Yes | Yes | Has touch switch interface | 483 |
| ITT Semiconductor | 7150 | PMOS | ? | ? | N.A.[1] | ? | ? | 25 | Yes | ? | ? | ? | ? | ? | ? | 14 | Yes | 14/18/24 | −15 | No | No | No | No | Designed for washing machines | 484 |
| National Semi | MM57109 | PMOS | 4/8 | 5×32 | N.A. | Yes | 70 | 400 | No | 1220/1 S | Yes | Yes | Yes/1 | 4 | 1 | 11 | Yes | 28 | 9 | No | No | No | No | Has scientific calculation ability | 485 |
| | MM57140/57152 | PMOS | 4/8 | 55×4 | 630×8 | No | 35 | 280 | Yes | 16/16 | Opt. | Yes | 0 | 2 | 4 | 24 | No | 28 | 7.9 to 9.5 | Yes | Yes | No | Yes | Drives LEDs or fluorescents | 486 |
| | MM5799 | PMOS | 4/8 | 96×4 | 1536×8 | No | 35 | 400 | Yes | 10/20 | Opt. | Yes | 0 | 2 | 5 | 23 | Yes | 28 | 7.9 to 9.5 | Yes | Yes | No | Yes | Serial I/O and LED drive | 487 |
| | MM5781/82 | PMOS | 4/8 | 160×4 | 2048×8 | Yes | 35 | 400 | No | 10/20 | Opt. | Yes | 0 | 2 | 5 | 24 | Yes | 28 | 7.9 to 9.5 | Yes | Yes | No | Yes | Two chip set | 488 |
| NEC Microcomputers | μPD548 | PMOS | 4/10 | 96×4 | 1920×10 | Yes | 72 | 200 | No | 10/20 | Yes | Yes | Yes/2 | 4 | RAM | 35 | No | 42 | −10 | Yes | Yes | No | No | Can interface to keyboard | 489 |
| | μPD546 | PMOS | 4/8 | 96×4 | 2000×8 | No | 80 | 440 | No | 10/40 | Yes | Yes | Yes/1 | 3 | 6 | 35 | No | 42 | −10 | Yes | Yes | No | Yes | Has 6-bit programmable timer | 490 |
| | μPD547 | PMOS | 4/8 | 64×4 | 1000×8 | No | 58 | 440 | No | 10/40 | Yes | Yes | Yes/1 | 1 | RAM | 35 | No | 42 | −10 | Yes | Yes | No | Yes | Instructions are 546 subset | 491 |
| | μPD545 | PMOS | 4/8 | 32×4 | 640×8 | No | 58 | 440 | No | 10/40 | Yes | Yes | Yes/1 | 1 | RAM | 21 | No | 28 | −10 | Yes | Yes | No | Yes | Can handle high voltages | 492 |
| Rockwell | PPS-4 | PMOS | 4/8 | 0 | 0 | Yes | 50 | 200/400 Two clocks | No | 5/15 | No | Yes | Yes/1 | 2 | 1 | 12+ | Yes | 42 | −17/+5,−12 | Yes | Yes | No | Yes | Combination ROM/RAM/I/O available | 493 |
| | PPS 4/2 | PMOS | 4/8 | 0 | 0 | Yes | 50 | 200/400 | Yes | 5/15 | No | Yes | No | 2 | 1 | 12+ | Yes | 42 | −17/+5,−12 | Yes | Yes | No | Yes | Same as PPS-4 but has internal clk | 494 |
| | PPS-4/1 MM77 | PMOS | 4/8 | 96×4 | 1344×8 | RAM only | 50 | 100/4 | Yes | 10/40 | Yes | Yes | Yes/1 | 2 | 2+RAM | 31 | Yes | 42 | −15/+5,−10 | Yes | Yes | No | Yes | I/O includes serial channel | 495 |
| | MM78 | PMOS | 4/8 | 128×4 | 2048×8 | RAM only | 50 | 100/4 | Yes | 10/40 | Yes | Yes | Yes/1 | 2 | 2+RAM | 31 | Yes | 42 | −15/+5,−10 | Yes | Yes | No | Yes | Software compatible with 77 | 496 |
| | MM76 | PMOS | 4/8 | 48×4 | 640×8 | RAM only | 50 | 100/4 | Yes | 10/40 | Yes | Yes | Yes/1 | 1 | 1+RAM | 31 | Yes | 42 | −15/+5,−10 | Yes | Yes | No | Yes | Primarily used for keyboard display | 497 |
| | MM76/C | PMOS | 4/8 | 48×4 | 640×8 | RAM only | 50 | 100/4 | Yes | 10/30 | Yes | Yes | Yes/1 | 1 | 1+RAM | 39 | Yes | 52 | −15/+5,−10 | Yes | Yes | No | Yes | Has high-speed counter | 498 |
| | MM76/D | PMOS | 4/8 | 48×4 | 640×8 | RAM only | 50 | 100/4 | Yes | 10/30 | Yes | Yes | Yes/1 | 1 | 1+RAM | 37 | Yes | 52 | −15/+5,−10 | Yes | Yes | No | Yes | Has a/d converter on chip | 499 |
| | MM76/E | PMOS | 4/8 | 48×4 | 1024×8 | RAM only | 50 | 100/4 | Yes | 10/30 | Yes | Yes | Yes/1 | 1 | 1+RAM | 31 | Yes | 42 | −15/+5,−10 | Yes | Yes | No | Yes | Larger ROM than MM76 | 500 |
| | MM76/L | PMOS | 4/8 | 48×4 | 640×8 | RAM only | 50 | 100/4 | Yes | 10/30 | Yes | Yes | Yes/1 | 1 | 1+RAM | 31 | Yes | 40 | 6 to 11 | Yes | Yes | No | Yes | Low voltage version of 76 | 501 |
| | MM75 | PMOS | 4/8 | 48×4 | 670×8 | RAM only | 50 | 100/4 | Yes | 10/40 | Yes | Yes | Yes/1 | 1 | 1+RAM | 22 | Yes | 28 | −15/+5,−10 | Yes | Yes | No | Yes | Reduced I/O version of 76 | 502 |
| Texas Instruments | TMS-1000 | PMOS/NMOS | 4/8 | 64×4 | 1024×8 | No | 43 | 400 | Yes | 15/15 | Yes | Yes | Yes/1 | 1 | 2 | 23/25 | Yes | 28/40 | 15 | Yes | Yes | Yes | Yes | Also a 35 V family available | 503 |
| | TMS-1100 | PMOS/NMOS | 4/8 | 128×8 | 2048×8 | No | 40 | 400 | Yes | 15/15 | Yes | Yes | Yes/1 | 1 | 2 | 23/28 | Yes | 28/40 | 15 | Yes | Yes | Yes | Yes | Pin compatible with TMS-1000 | 504 |
| | TMS-1018 | PMOS | 4/8 | 64×4 | N.A. | No | 43 | 400 | Yes | 15/15 | Yes | Yes | No | N.A. | N.A. | 4 | No | 28 | 15 | Dedicated number cruncher | | | | | 505 |
| | TMS-1117 | PMOS | 4/8 | 128×8 | N.A. | No | 43 | 400 | Yes | 15/15 | Yes | Yes | No | N.A. | N.A. | 19 | Yes | 28 | 15 | Dedicated controller for microwave ovens | | | | | 506 |
| Western Digital | 1872 | PMOS | 4/10 | 4×32 | 512×10 | No | 37 | 150 | Yes | 6.25/12.5 | Yes | Yes | Yes/1 | 1 | RAM | 27 | No | 40 | 12 | Yes | Yes | Yes | Yes | RAM holds BCD numbers | 507 |
| Fairchild 1 chip | Micromachine | NMOS | 8/8 | 64×8 | 2048×8 | Yes | 70+ | 4000 | Yes | 1/6.5 | Yes | Yes | Yes/4 | RAM | RAM | 32 | Yes | 40 | 5 | Yes | Yes | Yes | Yes | Software compatible with F8 | 508 |
| General Instrument | PIC-1650 | NMOS | 8/12 | 32×8 | 512×12 | Yes | 31 | 1000 | Yes | 4/8 | Yes | Yes | Yes/1 | 2 | RAM | 32 | No | 40 | 5 | Yes | Yes | Yes | Yes | Smaller I/O and larger ROMs avail | 509 |
| Intel | 8048/8748 | NMOS | 8/8 | 64×8 | 1024×8 | Yes | 96 | 6000 | Yes | 2.5/5 | Yes | Yes | Yes/1 | 8 | RAM | 27 | Yes | 40 | 5 | Yes | Yes | Yes | Yes | 8748 has uv PROM | 510 |
| Mostek 1 chip F-8 | 3870 | NMOS | 8/8 | 64×8 | 2048×8 | Yes | 70+ | 4000 | Yes | 1/6.5 | Yes | Yes | Yes/4 | RAM | RAM | 32 | Yes | 40 | 5 | Yes | Yes | Yes | Yes | Software compatible with F8 | 511 |
| Motorola | 6400 | NMOS | 8/8 | 32×8 | 1024×8 | Yes | ? | 8000 | Yes | ? | Yes | ? | ? | ? | RAM | ? | Yes | ? | 5 | Yes | 1978 | 1978 | 1978 | Intended for controller use | 512 |
| | 6801 | NMOS | 8/8 | ? | ? | Yes | ? | 2000 | ? | ? | Yes | ? | ? | ? | ? | ? | Yes | 40 | 5 | No | 1978 | 1978 | 1978 | Available 1978 | 513 |
| Rockwell | PPS-8 | PMOS | 8/8 | 0 | 0 | Yes | 100 | 256/4 | No | 4/12 | No | Yes | Yes/3 | 16 | 2 | 0+ | Yes | 42 | −17/+5,−12 | Yes | Yes | No | Yes | Combination RAM/ROM/I/O support | 514 |
| | PPS-8/2 | PMOS | 8/8 | 0 | 0 | Yes | 100 | 200/4 | No | 5/15 | No | Yes | Yes/3 | 16 | 2 | 0+ | Yes | 42 | −17/+5,−12 | Yes | Yes | No | Yes | I/O chip includes clock | 515 |
| Zilog | Z8 | NMOS | 8/8 | 96×8 | 2048×8 | Yes | ? | 4000 | Yes | 0.75/? | Yes | Yes | Yes/? | ? | RAM | 32 | Yes | 40 | 5 | 1978 | 1978 | 1978 | 1978 | Has two counter/timers | 516 |

1 Not applicable ? Not available

(continued on page 34)

New from Centralab...

# IMPS PUSHBUTTON SWITCHES

## A new miniature modular building block system that offers microprocessor control designers more of what they need.

To meet the special digital and analog needs of today's $\mu$P-based controls, Centralab offers design engineers a whole new system of modular pushbutton switch building blocks. We call it IMPS — Integrated Modular Panel System. IMPS saves PC board and panel area and simplifies front panel design, cuts assembly costs, reduces back-panel space requirements, and meets the digital-analog needs of $\mu$P-based controls. Check these space saving, cost-cutting features.

### Simplify front panel interface.

All IMPS switches regardless of function, are uniform in size, simplifying design and selection of front panel hardware. They have high volumetric efficiency, occupying .505" x .388" PC board area and require only .608" of space between PC board and front panel.

### Cut assembly costs.

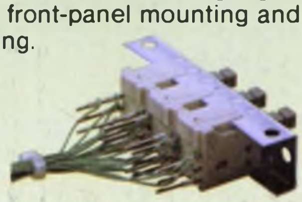
IMPS switches may be mounted on the front panel, and are designed for automatic wave soldering installation and PC board cleaning. Insert molded terminals prevent flux and solder wicking and contact contamination. Integral PC board stand-offs provide for efficient board cleaning.

### Meet analog and digital needs.

IMPS switches are available with momentary, push-push and interlocking actions, with a long-life contact system that switches both digital and analog signals. To accommodate critical signal requirements, housings are high-insulation molded plastic with UL 94V-0 rating.

### Available options.

Optional installations include ganged assemblies, front-panel mounting and wire-wrapping.



All IMPS pushbutton switches are built to Centralab's highest quality standards (see specifications at right). They're priced as low as 41 cents in 1,000 quantity. For full technical details, samples and quotation, call (515) 955-3770, or write to the address below.

### Built To Centralab Quality Specs.

IMPS Pushbutton Switches combine compact size, low cost and highest quality throughout.

- Silver or gold inlay wiping contacts for long-life and low-contact resistance.
- Less than 2 milliseconds contact bounce.
- SPST, SPDT, DPST, and DPDT switch contacts.
- Printed circuit, DIL socket or wire-wrap terminations available.
- 2.5 to 3.5 oz. actuation force (momentary).
- Choice of button interface — square or blade shaft (shown) — permits use of a variety of Centralab and industry standard buttons and keycaps.
- 10, 15, 20 or 25mm center-to-center spacing.

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**CIRCLE NUMBER 23**

# Table 3. Bit-slice families

| Company | Series | Process technology | ALU part number | ALU word size (bits) | Number of ALU instructions | Can ALU do BCD arithmetic | Maximum ALU clock rate (MHz) | General-purpose registers in ALU | ALU package size (DIP pins) | Microprogram sequencer number | Number of address bits | Maximum sequencer clock rate (MHz) | Number of sequencer commands | Sequencer stack size | Sequencer package size (DIP pins) | Are parts TTL compatible | Voltages required (V) | Prototyping system available | Development software available | Specialized support circuits available | Comments | Circle Number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Advanced Micro Devices | 2900 | STTL | 2901A | 4 | 64 | No | 10 | 16 | 40 | 2909/11 | 4 | 10 | 12 | 4×4 | 28/20 | Yes | 5 | Yes | Yes | Yes | Has widest number of second sources | 517 |
| Fairchild | Macrologic | STTL | 9405/34705 | 4 | 64 | No | 10 | 8 | 24 | 9406 | 4 | 10 | 4 | 16×4 | 24 | Yes | 5 | Yes | Yes | Yes | CMOS version (34705) operates at 2 MHz | 518 |
| | 100k 8-bit | ECL | ADIU | 8 | 27 | Yes | 20 | 1 | * | In definition stage | | | | | | | −4.5, −2 | 1978 | 1978 | 1978 | Only 8-bit slice | 519 |
| Intel | 3000 | STTL | 3002 | 2 | 40 | No | 10 | 11 | 28 | 3001 | 9 | 10+ | 11 | 0 | 40 | Yes | 5 | Yes | Yes | Yes | Only 2-bit ALU available | 520 |
| Monolithic Memories | 5700/6700 | STTL | 57/6701 | 4 | 32 | No | 5 | 16 | 40 | 6710 | 9 | 10+ | 8 | 0 | 40 | Yes | 5 | Yes | ? | No | Has double-addressing capability | 521 |
| Motorola | 10800 | ECL | 10800 | 4 | 100+ | Yes | 20 | 0 | 48 | 10801 | 4 | 20 | 16 | 4×4 | 48 | No | −2, −5.2 | Yes | Yes | Yes | Fastest bit slice available | 522 |
| National Semiconductor | IMP-4 | PMOS | 00A/520 | 4 | 8 | No | 5.714 | 20 | 24 | 4A/521 | 4 | 5.714 | 100+ | in ALU | 24 | Yes | +5, −12 | Yes | Yes | No | Need external register file | 523 |
| | IMP-8 | PMOS | 00A/520 | 4 | 8 | No | 5.714 | 20 | 24 | 8A/521 | 8 | 5.714 | 100+ | in ALU | 24 | Yes | +5, −12 | Yes | Yes | No | Uses IMP-4 ALUs with big ROM | 524 |
| | IMP-16 | PMOS | 00A/520 | 4 | 8 | No | 5.714 | 20 | 24 | 16A/521 | 16 | 5.714 | 100+ | in ALU | 24 | Yes | +5, −12 | Yes | Yes | No | Two development systems available | 525 |
| Texas Instruments | SBP-0400A | I²L | SBP 0400 | 4 | 512 | No | 5 | 10 | 40 | 74S482 | 4 | 20 | 64 | 4×4 | 20 | Yes | Current | Yes | No | No | Has pipeline register | 526 |
| | SBP-0401A | I²L | SBP 0401 | 4 | 512 | No | 5 | 10 | 40 | 74S482 | 4 | 20 | 64 | 4×4 | 20 | Yes | Current | Yes | No | No | Does not have pipeline register | 527 |
| | 74S481 | STTL | 74S481 | 4 | 24,780 | No | 10 | 0 | 48 | 74S482 | 4 | 20 | 64 | 4×4 | 20 | Yes | 5 | Yes | No | Yes | Very flexible instruction set | 528 |

*(continued from page 32)*

other processor, the 6802, will be a 6800 with an on-chip clock and 128 bytes of RAM. For easy use in power-down applications, 32 of the 128 bytes will be set aside for low-power operations.

Boosting operating speed is another ploy used by manufacturers to improve instruction execution time. Motorola has developed depletion-load versions of its 6800 to obtain 3 MHz clock rates and Signetics has done a redesign of its 2650 to obtain 2 and 2.5 MHz clock rates.

The 8X300 from Signetics is the only bipolar 8-bit microprocessor available aside from the SMS-300 from Scientific Microsystems. Both the 8X300 and SMS-300 use similar chips but the Signetics circuit has some slight differences in instruction operation and I/O capability.

The only 8-bit CMOS microprocessor, RCA's CDP1802, will soon have a little brother—the 1803. Little brother will have all the processing power of the 1802, but the number of I/O lines and control signals will be cut to squeeze the chip into a 28-pin DIP.

A high-performance version of the 1802, coming soon, will be made from silicon-on-sapphire and will be able to operate at even lower power levels and with better noise immunity.

For those demanding more performance from the standard 8080A, Intel responded with its 8085. In addition to containing nearly all the peripheral support circuits needed to make the 8080A run, the 8085 adds two new instructions to simplify interrupt handling. Following the trend, the 8085 operates from a single 5-V supply and has the clock circuit built onto the chip.

To keep the package size at 40 pins, however, the bus has been restructured so that instead of a separate 16-line address and 8-line data bus, the 8085 has an 8-line address bus and a multiplexed 8-bit data/address bus. Because these buses are unusual, several special peripheral circuits developed for them have no equal on the market: the 8155, a 256 × 8 static RAM with 14-bit counter/timer and 22 programmable I/O lines; and the 8355/8755, a 2048 × 8 ROM/UV EPROM with two parallel 8-bit ports.

The 8080A has also been "improved" by Advanced Micro Devices, NEC Microcomputers and even more so by Zilog. AMD offers a version, the 9080A, that has better bus driving capability while NEC's μPD 8080A is pin-compatible, but with a BCD subtraction instruction in addition to the normal

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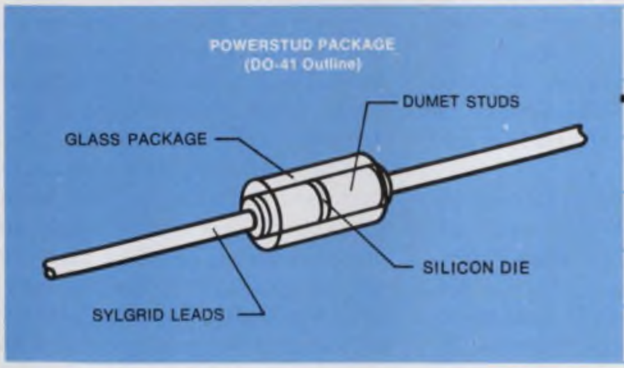
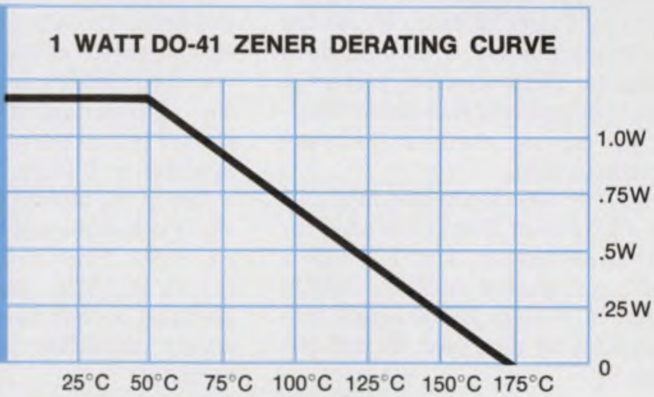
*Military types also available.

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CIRCLE NUMBER 24

8080A command set.

Zilog's Z80, introduced as a souped up 8080A, is the only CPU that is code-compatible with the 8080A or 8085. It also has many of the support circuits built in, operates from a 5-V supply and has about 80 more instructions. Now, a 4-MHz version of the original 2 MHz CPU is being offered, and industry rumors say that Zilog is hard at work on a higher-performance design.

### Larger words, better performance

Beyond the 8-bit size, relatively few processors are available. Two of them are 12-bit μPs—the IM6100 from Intersil and the T3190 from Toshiba. The 6100, in addition to the RCA 1802, completes the list of CMOS processors and effectively exploits existing software for the Digital Equipment Corp. PDP-8. Most PDP-8 code can run on the 6100 directly, and CMOS construction yields an operating power down in the milliwatt range.

Toshiba's 12-bit processor, available in PMOS or NMOS, offers over 100 instructions—including multiplication and division—and comes in a 36-pin DIP. With multiply and divide commands built in, the T3190 provides a versatile instruction set and can save a tremendous amount of processing time where mathematical operations are required. Moreover, it is the only microprocessor with a word length less than 16 bits that offers hardware multiply and divide.

Only half a dozen 16-bit microprocessors are available from about as many companies. The Mn601 MicroNova processor from Data General uses existing Nova software, while the TMS-9900 from Texas Instruments uses software from its Series 990 mini. While an I²L processor is being developed by Fairchild that can use the Nova instruction set, a legal battle is ensuing as Data General presses a patent infringement suit against Fairchild for copying the Nova software and architecture.

The TMS-9900 chip is also available in an I²L version that is intended for harsh environments and for higher speed requirements than the NMOS version. A 10-MHz I²L processor will be available by next year, TI officials predict.

To allow for all the control signals and the dual 16-line buses, the TMS-9900 was packaged in a 64-pin DIP. But when some customers balked, because of its incompatibility with insertion tools and the difficulty of obtaining sockets, Texas Instruments redesigned the TMS-9900 μP to fit in a 40-pin DIP—the TMS-9980. The data and address buses are multiplexed and the number of interrupt levels is down. Even so, the TMS-9980 is totally software-compatible with the TMS/SBP-9900 parts.

General Instrument also decided to multiplex its data and address buses to squeeze the chip into a 40-pin DIP. A recently introduced slower version of the CP1600, called the CP1610, is housed in a 40-pin plastic package and operates at 2 MHz.

One of the oldest 16-bit processors is the PACE developed by National Semiconductor. Since it's built from PMOS, it runs at 2 MHz, max. However, it is designed to handle BCD arithmetic, which simplifies man/machine interfaces.

There aren't many newcomers to the 16-bit field. Motorola is supposedly readying a 16-bit μP to be introduced in late 1978 or early 1979.

Panafacom, a Japanese combine, consisting of Fujitsu, Matsushita and Fuji Electric, developed a processor called the L-16A (Mn1610) over a year ago. But little is known about it outside Japan. A 16-bit that was being planned by MOS Technology earlier this year has been shelved.

## Second source reference by processor type

| Type number | Original manufacturer | Second sources |
|---|---|---|
| 2900 series | Advanced Micro Devices | Motorola, National Semiconductor, Raytheon, Sescosem, Signetics, Fairchild |
| F-8 (2 chip) | Fairchild | Mostek, SGS-ATES |
| 3859 | Fairchild | |
| Macrologic | Fairchild | Signetics |
| CP1600 | General Instrument | EM&M Semi |
| 1650 | General Instrument | EM&M Semi |
| 8000 | General Instrument | AEG and SGS/ATES |
| 3000 series | Intel | Signetics |
| 4001 series | Intel | National Semiconductor |
| 8080A | Intel | Advanced Micro Devices, NEC, National Semiconductor, Signetics, Texas Instruments |
| 6100 | Intersil | Harris Semiconductor |
| 6700 series | Monolithic Memories | |
| 65XX | MOS Technology | Rockwell, Synertek |
| 3870 | Mostek | Motorola |
| 6800 | Motorola | American Microsystems, Fairchild, Fujitsu, Hitachi, Sescosem/Thompson CSF |
| PACE | National Semiconductor | Rockwell |
| SC/MP II | National Semiconductor | Rockwell, Signetics, Western Digital |
| 1802 | RCA | Hughes, Solid State Scientific |
| PPS-4,8 | Rockwell | National Semiconductor, Sharp (Tokyo) |
| SMS-300 | Scientific Microsystems | Signetics (8X300) |
| 2650 | Signetics | Advanced Memory Systems, National Semiconductor |
| Z80 | Zilog | Mostek, Sharp (Tokyo) |

### Make your micro with slices

However, if going through the many manufacturers' advertising and data sheets doesn't uncover the right processor, available standard logic or Schottky and ECL bipolar bit-slice circuits can be used to build one. Such circuits offer fast cycle times for most instructions and even though much more circuitry is required, they can be microprogrammed to perform any instruction. The earliest bit-slice processor, National Semiconductor's IMP-4, 8 and 16 series, is fabricated from PMOS.

The *de facto* standard bipolar bit slice seems to be Advanced Micro Devices' 2900 series. With over six alternate sources, it is the most widely imitated processor product available. (For more details about the 2900 family

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see Microprocessor Basics: Part 14, ED No. 10, May 10, 1977 p. 62.)

Predating the 2900, though, is the 2-bit bit slice developed by Intel—the Series 3000. Although not as popular as the 2900, the Series 3000 slices permit very flexible processor design —any word size from 2 to n × 2 bits can be made.

The 10800 family made by Motorola offers the fastest cycle times of any available bit slice—with maximum clock rates of 15 MHz, the cycle time reaches a swift 70 ns. The ALU section can handle BCD calculations as well as normal binary manipulations—a feature no other bit-slice currently has. However, Advanced Micro Devices is working on an improved version of the 2901A ALU that includes multiplication and division instructions as well as the capability to handle floating-point arithmetic routines. This enhanced chip, dubbed the 2903, is expected to be available later this year.

Just two other bit slice series are available—and they're both from Texas Instruments. The older chip is the SBP-0400 or 0401A 4-bit slice. Both versions are fabricated with $I^2L$. The only difference between the two is that the 0400A includes an extra register that permits pipeline operation to speed up instruction execution.

Recently introduced by TI, however, is a family of Schottky-TTL slices called the 74S481 series. The ALU offers almost 25,000 possible instructions (some of the commands are redundant) and comes in a 48-pin package. The processors will probably fill the same applications as the Macrologic series of Schottky-TTL parts recently introduced by Fairchild. Although not offering as many instructions as the 74S481, Fairchild's 9405 ALU comes in a package half the size—24-pin.

To help keep power dissipation low in applications that don't call for top speed, Fairchild offers CMOS equivalents to some of its Macrologic parts to help keep power dissipation low. The CMOS ALU operates at a maximum clock or 2 MHz. But for the tops in speed, Fairchild may have the solution next year—an ECL bit slice with an 8-bit data word. No part number has yet been assigned, but the ALU chip has been given the temporary name of Arithmetic Data Input Unit (ADIU).

The ADIU is expected to handle instructions in a 50-ns cycle and do error-correction code operations and parity checking when the chips are set up for a 32-bit word size. Because of the large word size of each ADIU section, a 64-contact leadless ceramic package has been designed to handle the circuit and its heat dissipation requirements.■■

## Need more information?

Listed below are the original-source microprocessor manufacturers and most of the alternate source vendors. For additional companies consult ELECTRONIC DESIGN's Gold Book under IC, Central Processing Unit and Computers, Digital, Micro.

Advanced Memory Systems, 1215 Hammerwood Rd., Sunnyvale, CA 94086. (408) 734-4330. **Circle No. 552**

Advanced Micro Devices, 901 Thompson Pl., Sunnyvale, CA 94086. (408) 732-2400. **Circle No. 529**

American Microsystems, 3800 Homestead Rd., Santa Clara, CA 95051. (408) 246-0330. **Circle No. 553**

Data General, Route 9, Southboro, MA 01772. (617) 485-9100. **Circle No. 530**

Essex International, 564 Alpha Dr., Pittsburgh, PA 15238. (412) 782-0200. **Circle No. 531**

Fairchild, 1725 Technology Dr., San Jose, CA 95110. (408) 998-0123. (MOS) **Circle No. 532**

Fairchild Semiconductor, 464 Ellis St., Mountain View, CA 94042. (415) 962-3816. (Bipolar) **Circle No. 554**

Ferranti Ltd., Western Rd. Bracknell, Berkshire RG12 1RA, England **Circle No. 533**

General Instrument, 600 W. John St., Hicksville, NY 11802. (516) 733-3130. **Circle No. 534**

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901. (305) 727-5400. **Circle No. 555**

Hughes Microelectronics, 500 Superior Ave., Newport Beach, CA 92662. (714) 548-0671. **Circle No. 556**

ITT Semiconductor, 74 Commerce Way, Woburn, MA 01801. (617) 935-7910. **Circle No. 535**

Intel, 3065 Bowers Ave., Santa Clara, CA 95051. (408) 246-7501. **Circle No. 557**

Intersil, 10900 N. Tantau Ave., Cupertino, CA 95014. (408) 996-5000. **Circle No. 536**

MOS Technology, Valley Forge Corporate Center, 950 Rittenhouse Rd., Norristown, PA 19401. (215) 666-7950. **Circle No. 537**

Monolithic Memories, 1165 E. Arques Ave., Sunnyvale, CA 94086. (408) 739-3535. **Circle No. 538**

Mostek, 1215 W. Crosby Rd., Carrollton, TX 75006. (214) 242-0444. **Circle No. 539**

Motorola Semiconductor, 3501 Ed Bluestein Blvd., Austin, TX 78721. (512) 928-2600. (MOS) **Circle No. 540**

Motorola Semiconductor, 5005 E. McDowell Rd., Phoenix, AZ 85008. (602) 244-6900. (Bipolar) **Circle No. 558**

NEC Microcomputers, 5 Militia Dr., Lexington, MA 02173. (617) 862-6410. **Circle No. 541**

National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95050. (408) 737-5000. **Circle No. 542**

Panafacom Ltd., 2-10-16 Jiyuzaoka, Mezuro-ku Tokyo, Japan 152. **Circle No. 543**

RCA, Box 3200, Route 202, Somerville, NJ 08876. (201) 685-6423. **Circle No. 544**

Raytheon, 350 Ellis St., Mountain View, CA 94040. (415) 968-9211. **Circle No. 559**

Rockwell International, P.O. Box 3669, RCOI-Dept 720, Anaheim, CA 92803. (714) 632-2321. **Circle No. 545**

Scientific Microsystems, 520 Clyde St., Mountain View, CA 94043. (415) 964-5700. **Circle No. 546**

Signetics, 811 E. Arques Ave., Sunnyvale, CA 94086. (408) 739-7700. **Circle No. 547**

Solid State Scientific, Montgomeryville Industrial Park, Montgomeryville, PA 18936 (215) 855-8400. **Circle No. 560**

Synertek, 3050 Coronado Dr., Santa Clara, CA 95051. (408) 241-4300. **Circle No. 561**

Texas Instruments, 13500 North Central Expressway, Dallas, TX 75222. (214) 238-2481. **Circle No. 548**

Toshiba Transistor Works, 1 Komukai Toshiba-cho, Kawasaki-shi Kanagana-ken, Japan. **Circle No. 549**

Western Digital, 3128 Red Hill Ave., Newport Beach, CA 92663. (714) 557-3550. **Circle No. 550**

Zilog Microcomputers, 10460 Bubb Rd., Cupertino, CA 95014. (408) 446-4666. **Circle No. 551**

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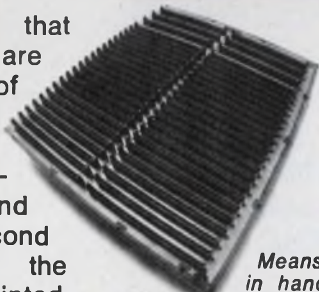

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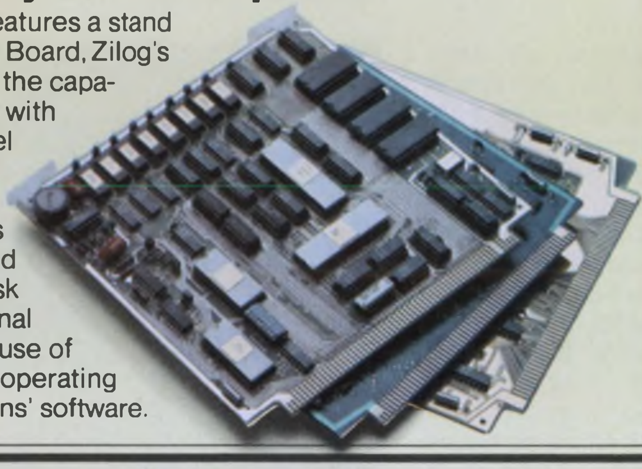


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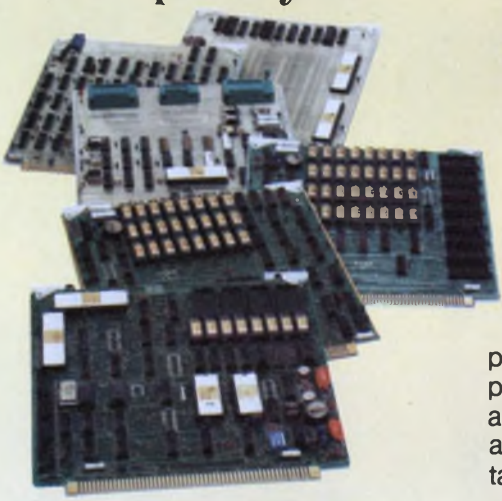

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- Z80-PMB PROM Memory Board: Contains sockets for up to 32K bytes of EPROM or PROM and additional programmable I/O channels.
- Z80-PPB PROM Programmer Board: Allows the user to program PROM's or EPROM's electrically.
- Z80-SIB Serial I/O Board: Provides additional four (4) serial duplex channels.
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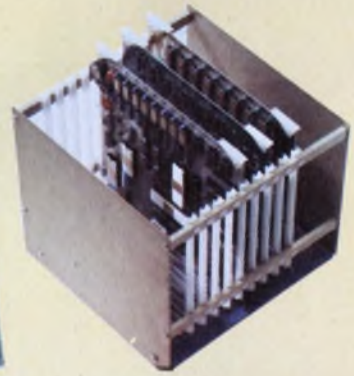

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**CIRCLE NUMBER 31**

# Washington report

## B-1 heads list of key defense budget issues

The B-1 bomber heads the list of 32 key defense issues slated for review by the Office of Management and Budget (OMB) during the current preparation of the Pentagon's fiscal 1979 budget. The budget will be submitted next January for the fiscal year beginning Oct. 1, 1978, but the major programs are being shaped now in talks involving President Carter, Defense Secretary Harold Brown and OMB Director Bert Lance.

The B-1, which is now projected to cost \$100-million each in production, is being considered for a stretch-out or outright cancellation. The Air Force had requested 244 of the bombers, but the final number may drop to 155, if President Carter agrees to production, according to Congressional supporters of the program.

Other issues concerning industry include possible slow-down or cancellation of the MX missile and Trident submarine/missile programs and the future of cruise missiles. In addition, all military command, control and telecommunications programs, along with defense research activities and the practice of contracting out support services will be examined.

## Proposal requests due for new Navy RPV

Finally, after a year's delay, the Navy expects to seek proposals from industry this summer for a new remotely piloted vehicle (RPV) that can be launched from small destroyers to spot targets for the Harpoon anti-ship missile, then recovered. Known as the over-the-horizon (OTH) RPV, the program has been stalled by funding problems and the Navy's inability to establish priorities in the area of unmanned drone aircraft. But now, after a series of studies, the top priority is OTH targeting, followed by tactical reconnaissance.

At least four companies—Boeing, Lockheed Missiles & Space Co., Northrop Ventura (CA) Div. and Rockwell International Columbus (OH) Div.—are preparing bids for the OTH competition. While their approaches vary, all four will have a range of about 100 miles, operate at subsonic speed, and probably carry infrared sensors for all-weather, day and night operation. The major technical problem is how to recover the RPVs safely.

Expandable RPVs would probably cost too much, according to the Navy. The airframe and engine are expected to cost \$25,000, which, could probably be cut in half if the RPVs didn't have to be recovered. But the basic \$100,000 avionics cost per vehicle would remain the same.

## Navy to continue Transit navsat series

A series of five improved Transit navigation satellites is planned by the Navy to be a guidance aid to its submarine-launched ballistic missiles. The first one is expected to be launched in the fall of 1979.

The 367-lb spacecraft will be launched on a four-stage Scout vehicle into an initial polar orbit of $194 \times 397$ nautical miles and then circularized at 600 nautical miles. The transmitting system consists of dual 5-MHz oscillators, phase modulators, transmitters operating at 400 MHz and 150 MHz, dual incremental phase shifters for controlling oscillator offset, and dual pseudorandom noise generators for superimposing data on the signals.

The onboard computer will be programmable from the ground and have enough memory for storing five days' worth of navigation messages. The combined capacity of the dual memory (262,144 bits in each) may be used to store a 10-day message. Normal readout rate is 50 bits/s, and the high-speed dump rate 1300 bps.

The command system consists of redundant receivers operating at 10 bps and 100 bps, command logic, power switching, low-voltage sensing switches and antennas. The telemetry system is digital and has a capacity for 172 channels of 8-bit words that can be read out directly at 325 bps or stored in memory. A back-up analog readout can be obtained on command via a voltage-controlled oscillator.

Four solar panels covered with solar cells and one 12 ampere-hour battery consisting of 12 NiCd cells comprise the power system. Nominal voltage is 16 V and power is 80 to 105 W.

RCA Astro-Electronics Div., which worked with the Applied Physics Laboratory of Johns Hopkins University on the original Transit series, is under contract for initial designs of the new version. The Navy plans to award a production contract to RCA for the first three this summer and another contract for two more in fiscal year 1980. The satellites are expected to operate until 1990.

The Air Force is having cost-overrun problems with its Navstar global positioning satellites, which are supposed to replace the current Transit Satellites. The Navy has been a participant in that program, but has been reluctant to accept Navstar until it is fully operational and has demonstrated that it is as reliable as Transit.

## FAA uses radar-checkout program to find lost aircraft

A computer program originally developed to check out the Federal Aviation Administration's air-traffic control systems has helped locate 31 aircraft downed in remote areas over the past two years—and in the first four months of this year alone.

The program was initially intended to check out the en-route radar systems that provide flight controllers with aircraft identity and altitude. But two years ago controllers at the FAA's Denver Air Route Traffic Control Center suggested that it could also help locate downed aircraft. They worked out the procedures in cooperation with the Air Force Rescue Coordination Center, Scott Air Force Base, IL.

Radar data on aircraft tagets are recorded on tape and retrieved for analysis in the form of a computer printout, which provides position data on all aircraft appearing on the radar screen at any given period. The current program is usable at 15 of the 20 control centers, but the FAA is rewriting the program to make it simpler. It is expected to be operating at all 20 centers in two years.

**Capital Capsules:** **The Navy is planning to upgrade the Phoenix long-range air-to-air missile** and purchase 465 of the improved versions by 1982, according to closed-door testimony recently released by the Senate Armed Services Committee. The Hughes-built missile is used on the F-14 fighter and is believed to be the only effective weapon against the high-flying, supersonic MIG-25 Foxbat. It also is being considered to counter the Soviet Backfire bomber. . . .**The future of the Compass Cope high-altitude reconnaissance drone hinges on joint U.S.-West German development of a new side-looking airborne radar,** designated the UPD-X, the Air Force told the same committee. The Air Force, which plans to spend $187-million to develop the huge drone, estimates that 40 of them would cost $408-million to produce. . . .**High-energy laser weapons will be tested by all three military services** at White Sands Missile Range, New Mexico, a site selected by the Defense Dept. The Navy had originally held out for its own site at San Juan Capistrano, CA. . . .The Air Force plans to launch studies in September of the RF-X advanced, all-weather tactical reconnaissance aircraft, which is reportedly another version of the F-15 fighter. Production will not be decided on until mid-1983.

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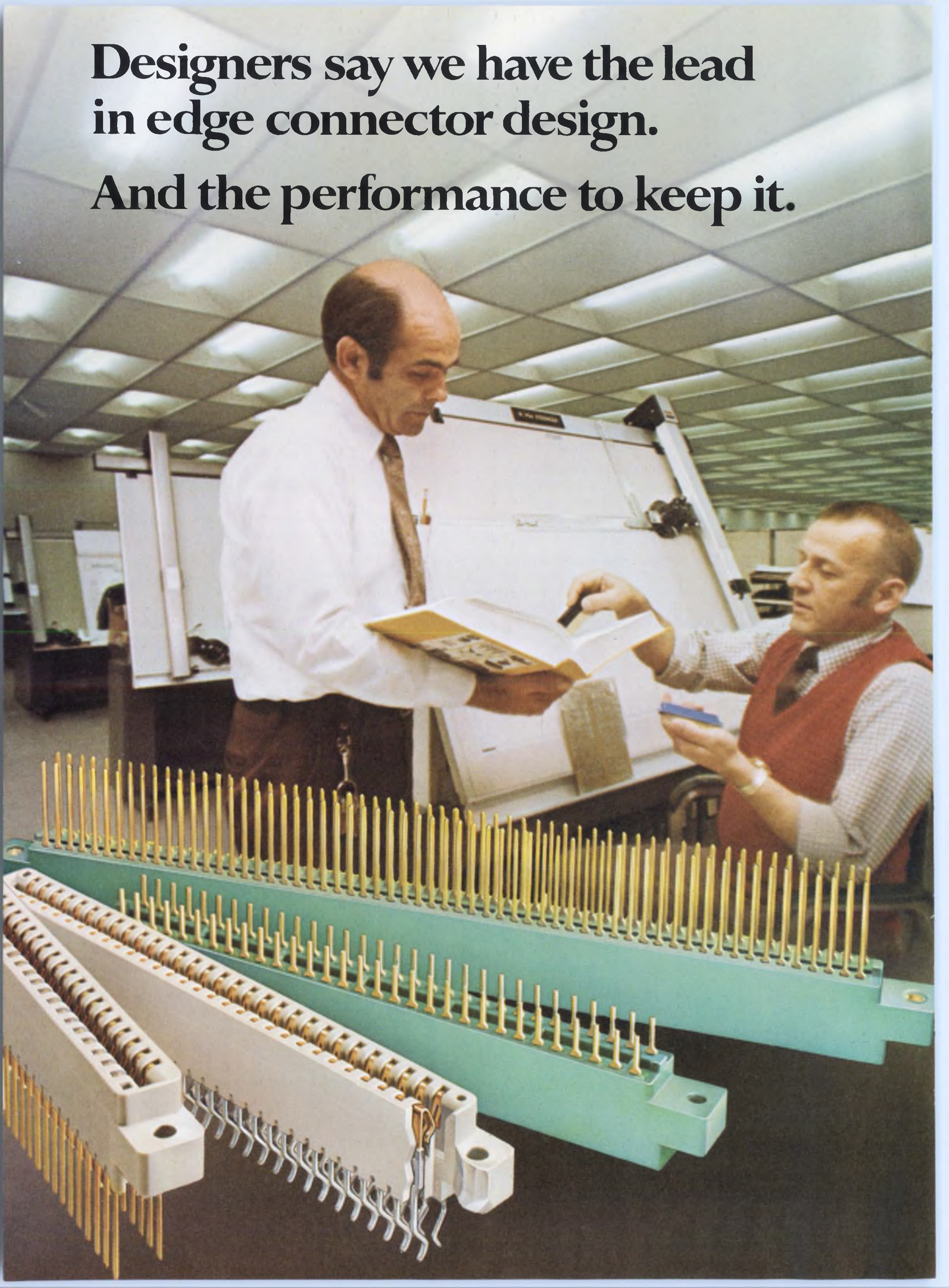
**CIRCLE NUMBER 33**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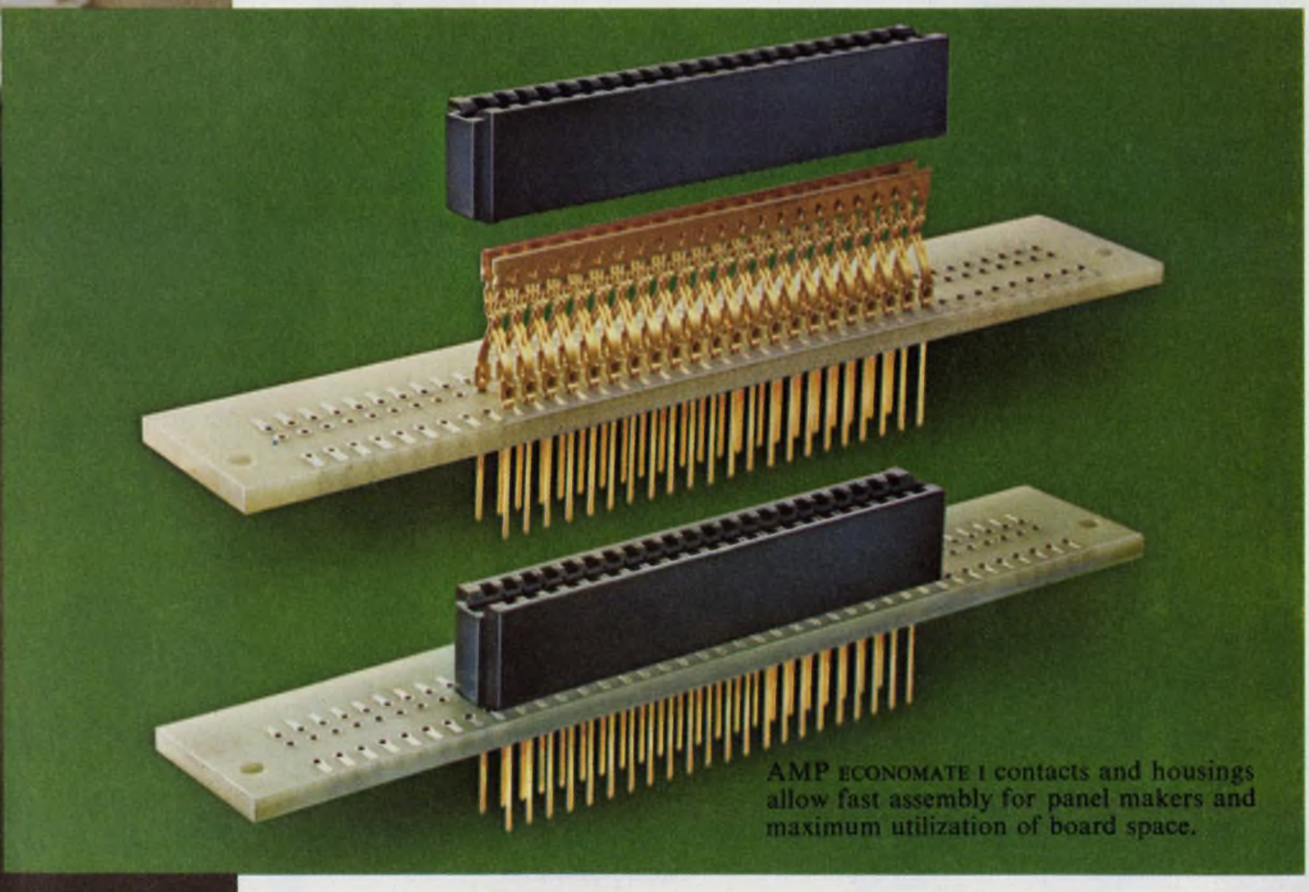

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| $\Delta E_{OS}/\Delta T$ ($\mu$V/°C), max. | 10 | 5 | 2 |
| $E_{OS}$ @25°C (mV), max. | 0.5 | 0.25 | 0.25 |
| Price (100's) | $7.95 | $10.35 | $19.40 |

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CIRCLE NUMBER 35

# Editorial

# Trimming the fat

Charlie had read many management books and attended many management seminars. And he had learned a basic lesson. He learned that reducing cost has far more effect on bottom-line net profit than increasing sales.

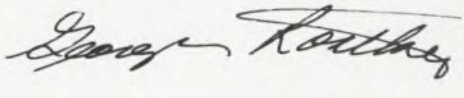
So Charlie started to search for cost centers, and he found them. He found, for example, that one secretary served every four engineers. Realizing that engineers don't have to write *that* many letters he cut the number of secretaries. And his profit margins grew. He found, too, that one technician served every three engineers. Since his engineers were getting too haughty anyway, Charlie felt it would bring them down a peg or two if they did their own breadboarding, wiring and testing. So he let go some of the technicians. And his profit margins grew. Then he realized that purchasing people were basically servants to the engineers, who made the real purchasing decisions while the purchasing people merely took care of the paperwork. Heck, he decided, let the engineers take care of their own paperwork. So he discharged some of the purchasing agents. And his profit margins grew.

Understandably, Charlie was delighted. He was just beginning to trim the fat in his organization. Just think of the profits that could develop when he started *really* looking for cost centers.

Charlie was like the man who had dropped 4500 feet from a plane flying at 5000. So far, everything was okay. But then there were some events that had not been predicted in the management texts because they were too obvious. Many things happened very slowly or not at all. The engineers couldn't spend much time designing newer products because they were too busy wiring and testing older designs. And they didn't always take advantage of the newest components because they didn't have time to organize vendor visits. They were also busy filing things and digging things out of their files and, on occasion, trying to type letters and reports.

So customers started to become unhappy and sales declined. Thanks to Charlie's cost-cutting measure, profit margins were up. But profits were down. This was disappointing and, unfortunately, it hadn't been stressed in management books because it was obvious. We all know that 6% is better than 5%. But 6% of $20 million isn't as nice as 5% of $25 million.

Charlie was ready for that. "We'll just cut some more cost," he said, "maybe, even, use cheaper components."



GEORGE ROSTKY
Editor-in-Chief

# Rockwell one-chip computers give you the right fit at the right price.

# Right now.

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All of Rockwell's one-chip computers offer powerful, user-oriented I/O ports that eliminate costly interface circuitry in overall systems.

I/O features, including bidirectional ports, flexibly designed drivers and receivers, and serial input/output ports, provide you with powerful system options.

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## Rockwell flexibility assures cost-effective design.

Rockwell's one-chip computers give you design options you couldn't afford with other logic approaches.

During the design stage you can add or reduce functions, allocate I/O differently and make dozens of other changes by simple reprogramming or by moving to another software-compatible chip within the family.

## Powerful instruction sets increase efficiency.

Rockwell's instruction sets provide ROM efficiencies of typically 2 to 1 over other microcomputers. For example, some one-byte multi-function Rockwell instructions perform operations requiring five instructions in other systems.

More than 80% of Rockwell's instruction types can be executed in one byte and in a single cycle. Special ROM instructions allow many subroutine calls to be handled in one byte. Table look-up instructions for MM77 and MM78 chips provide easy look up of stored data and easy keyboard decoding with minimal programming.

## The PPS 4/1 family of one-chip computers.

| Model | MM76 | MM77 | MM78 | MM75 | MM76C | MM76D | MM76E |
|---|---|---|---|---|---|---|---|
| Description | Basic 76 | Basic 77 | Jumbo 77 | Economy 76 | High speed counter* | 12-bit A/D converter | Expanded 76 |
| ROM (x8) | 640 | 1344 | 2048 | 640 | 640 | 640 | 1024 |
| RAM (x4) | 48 | 96 | 128 | 48 | 48 | 48 | 48 |
| Total I/O lines | 31 | 31 | 31 | 22 | 39 | 37 | 31 |
| Cond. Interrupt | 2 | 2 | 2 | 1 | 2 | 2 | 2 |
| Parallel Input | 8 | 8 | 8 | 4 | 8 | 8 | 8 |
| Bidirectional Parallel | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| Discrete | 10 | 10 | 10 | 9 | 10 | 10 | 10 |
| Serial | 3 | 3 | 3 | – | 3 | 3 | 3 |
| In-line package | 42 pin quad | 42 pin quad | 42 pin quad | 28 pin dual | 52 pin quad | 52 pin quad | 42 pin quad |
| Availability | Now | Now | Now | 2Q 77 | 2Q/77 | 3Q 77 | 16 wk ARO |

Power supply is 15v except low voltage version of Basic 76 available 3Q 77.
Typical power dissipation is 70mw.
*Two 8-bit or one 16-bit presetable up/down counter with 8 control lines.

## Rockwell design aids also help lower your system cost.

To help control development costs, Rockwell makes available a universal Assemulator that lets you assemble, edit, develop and debug programs, as well as load PROMs. Special development circuits enable prototyping.

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**Rockwell International**

# Get powerful microprocessor performance

## by using the Z80. With 158 instructions it offers more flexibility than other μPs, plus 8080 code compatibility.

The Z80 8-bit microprocessor combines all the processing power of the 8080 with 80 additional instructions. And to keep chip count to a minimum, many of the peripheral circuits necessary for 8080 systems have been built into the Z80. All members of the Z80 family are built with n-channel, silicon-gate, depletion-load technology; function at single-phase clock rates of 4 MHz; require just a 5-V supply; and have TTL-compatible inputs and outputs.

The circuit family consists of the Z80-CPU and the following peripherals: a counter-timer circuit (CTC), a parallel input/output circuit (PIO), a direct-memory-access controller (DMA), and a serial input/output circuit (SIO), as well as a group of support boards (Table 1). All the circuits are available in 2.5 or 4-MHz versions, ceramic packages, and extended temperature ranges. All are housed in 40-pin DIPs, except the CTC, which comes in a 28-pin DIP.

All peripheral circuits can be daisy-chained for priority interrupt control. Since most peripheral circuits necessary for system operation are built into the Z80, a minimum system consists of the Z80, a system clock, a power-on reset circuit and any memory and peripheral circuits desired (Fig. 1). At the system level, the μP supports vectored priority-interrupt structures without any extra hardware.

### Interfaces to the Z80 are simple

Although the Z80 maintains timing and control-signal compatibility with the 8080, it is not pin-compatible. All output lines can sink 1.8 mA at 0.4 V—the equivalent of one standard TTL load.

Three major buses from the chip—the 16-bit address bus, the 8-bit bidirectional data bus and a 13-line control bus—account for 37 of the Z80's 40 pins (Fig. 2). The other three pins are for power, ground and the single-phase clock. Unlike the 8080, the Z80 needs no status latch or clock, and interrupt vectoring and dynamic-memory refresh are completely supported within the μP itself.

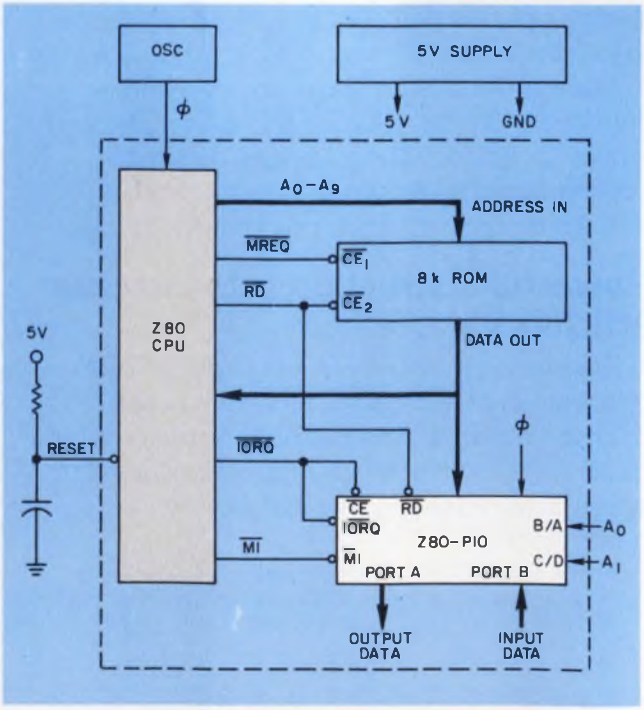
The 13 control lines are actually subdivided into three control buses: system control (six lines), μP

**Ralph Ungermann,** Vice President, and **Bernard Peuto,** Manager, Computer Architecture, Zilog, 10460 Bubb Road, Cupertino, CA 95014.

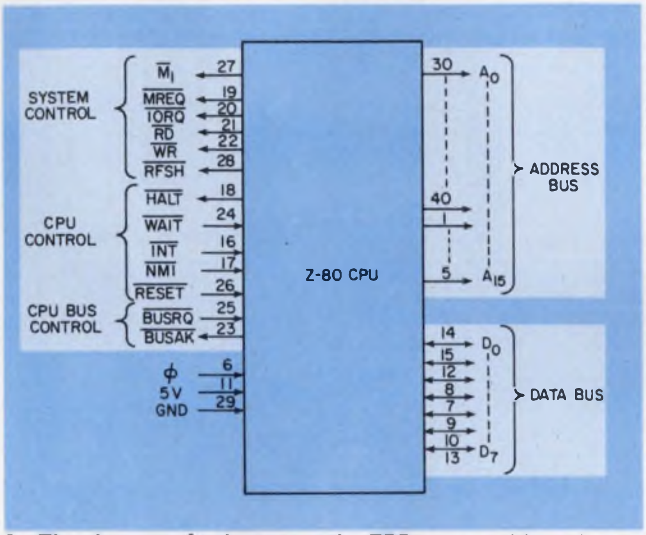
### Table 1. Z80 system components

| Part # | Description | Price ** 100 qty |
|---|---|---|
| Z80-CPU | 8-bit CPU, 2.5 MHz * | $26.50 |
| Z80-CTC | Counter/timer, 2.5 MHz * | $17.00 |
| Z80-PIO | Parallel I/O, 2.5 MHz * | $11.00 |
| Z80-DMA | Direct mem. access, 2.5 MHz * | $38.00 |
| Z80-SIO | Serial I/O, 2.5 MHz * | N.A. |
| | Support boards | unit qty |
| MCB | Microcomputer board—kit | $435. |
| | —assembled | $495. |
| MDC | Memory/floppy-disc controller | $795. |
| RMB | RAM memory board | $750. |
| IOB | Input/output board | $350. |
| PMB | PROM/ROM memory board | $395. |
| PPB/ EPROM | EPROM programmer (for 2708) | $475. |
| PPB/ PROM | PROM programmer (for 7620, 7640) | $475. |
| CPB/ ROM | Combination programmer | $575. |
| VDB | Video-display board | $475. |

* 4-MHz versions of these parts are available.
** 0 to 70-C ratings in plastic packages.




1. **A minimal Z80 system** can be built with the μP, an oscillator, some memory and an I/O port such as the PIO. Just a power supply and reset circuit must be added.




2. **The three major buses on the Z80** are an address bus, a data bus and a control bus. The control bus can be split into three smaller buses—one for system control, one for processor control and one for bus control.

control (five lines), and $\mu$P-bus control (two lines). One bus-control line functions as a bus-request line ($\overline{BUSRQ}$), which is an input that requests not only the $\mu$P's address and data buses, but also the memory-request, I/O-request, read-data and write-data lines of the system-control bus to go to a high-impedance state so that other devices can use the bus. The other bus-control line, an output signal called bus-acknowledge ($\overline{BUSAK}$), goes high to indicate when the lines go into a high-impedance third state.

All six system-control signals are outputs from the $\mu$P. An $\overline{M_1}$ line (machine cycle 1) goes Low to indicate when the $\mu$P is in the op-code-fetch part of an instruction. The memory-request line ($\overline{MREQ}$) goes Low when the address bus holds a valid address for a memory-read or write operation. An I/O-request line ($\overline{IORQ}$) goes Low to indicate that the lower byte of the address bus holds a valid I/O-port address for an I/O-read or write operation.

Memory-read and memory-write lines ($\overline{RD}$ and $\overline{WR}$) are also active when Low. $\overline{RD}$ indicates that the $\mu$P wants to read data from a memory or I/O device, while $\overline{WR}$ indicates that the data bus holds data to be stored in the addressed location. When the sixth system-control line, a refresh signal ($\overline{RFSH}$), goes Low, it indicates that the lower seven bits of the address bus contain a refresh address for dynamic memories, so the current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memory.

The five $\mu$P-control lines consist of one output signal and four input lines. All lines are active when Low. The only output is the halt line, which indicates when the $\mu$P has executed a software HALT instruction and is waiting for either a nonmaskable or maskable interrupt. While halted, the $\mu$P automatically executes NOP instructions to maintain the memory refresh. The wait input ($\overline{WAIT}$) indicates to the $\mu$P that the addressed memory or I/O device isn't ready for a data transfer (the $\mu$P will enter wait states for as long as this line is Low). This line allows memory or peripheral of any speed to be synchronized with the Z80.

To reset the $\mu$P or initialize it once it is on, the $\overline{RESET}$ line can be pulled Low. When pulled Low, it forces the Z80's program counter to $ØØ_{16}$, disables the interrupt-enable flip-flop, sets register I to $ØØ_{16}$, sets register R to $ØØ_{16}$, and sets the interrupt node to Ø.

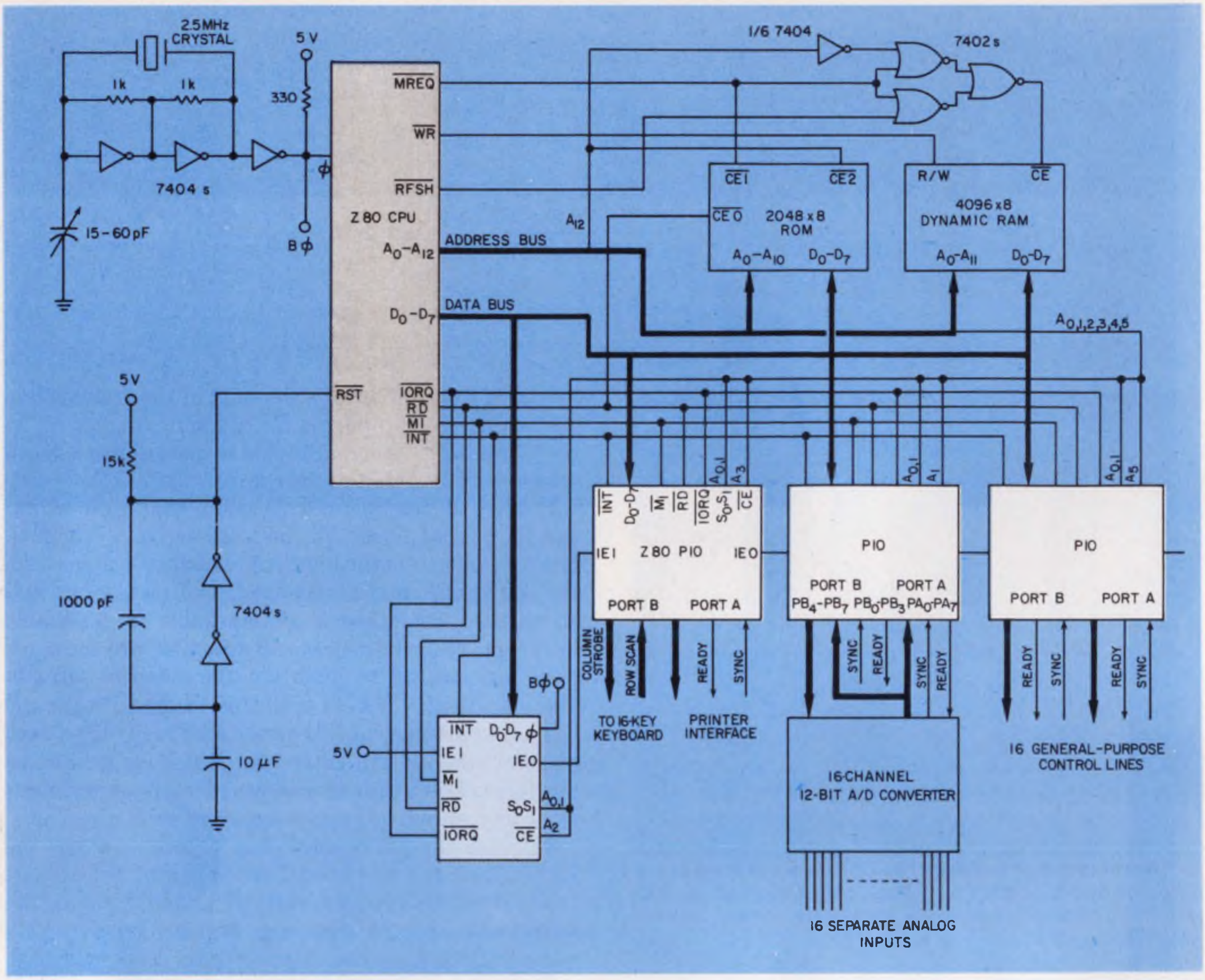
The last two lines are the interrupt-request ($\overline{INT}$) and nonmaskable-interrupt ($\overline{NMI}$) inputs. When pulled Low, the $\overline{INT}$ line interrupts the processor at the end of the current instruction if the software-controlled interrupt-enable flip-flop (IFF) is enabled, and if the $\overline{BUSRQ}$ line is High. Each time the $\mu$P accepts an interrupt, an acknowledge signal ($\overline{IORQ}$ during an $M_1$ time) is sent out at the beginning of the next instruction cycle.

The $\overline{NMI}$ line is a negative-edge triggered input, has a higher priority than the $\overline{INT}$ line, and is recognized at the end of the current instruction regardless of the IFF state. When triggered, it forces the Z80 to begin execution at location $ØØ66_{16}$ after saving the current contents of the program counter in an external stack.

### Interrupts and flags add flexibility

Three interrupt modes are available to the programmer. Mode Ø permits the interrupting device to insert any instruction on the data bus and have the $\mu$P execute it. Mode 1 has the $\mu$P automatically execute a restart to location $ØØ38_{16}$—no external hardware is required (the contents of the program counter are pushed onto the internal stack).

Mode 2, the most powerful, permits an indirect call




3. **By daisy-chaining the peripheral support circuits,** any number of peripheral chips can be added to this Z80-based process-control system. The device closest to the $\mu$P has the highest priority interrupt. Just 16 IC packages are needed to build this data-acquisition subsystem; and of the 16, nine are memories.

to any memory location. In this mode, the $\mu$P forms the indirect address from the upper byte of the I register and eight bits that are supplied by the interrupting device.

Two identical 8-bit flag registers (F and F′) are part of the Z80. Six of the bits in each register can be used as conditions for jump, call or return instructions; they are set or reset by various $\mu$P operations. Both the F and F′ registers have four testable flag bits and two nontestable bits. The four testable bits are the Carry flag, Zero flag, Negative-sign flag and Parity/overflow flag.

The Carry flag contains carry from the highest-order accumulator bit—add, subtract, shift and rotate instructions can alter its state. If an operation loads a zero into the accumulator, the Zero flag gets set. Otherwise, it is reset. Used with signed numbers, the Negative-sign flag gets set if the result of an operation is negative (bit 7 of the accumulator is the sign bit). The dual-purpose Parity/overflow bit gets set when the parity of the result in the accumulator for a logic operation is even, or is used to indicate overflow when signed 2's complement arithmetic is performed.

The two nontestable bits are Half-carry and Subtract flags. The Half-carry flag is a BCD-carry or borrow result from the least-significant four bits of the operation. (When a DAA instruction is used, this flag corrects the result of a previously packed decimal-add or subtract operation.) The Subtract flag corrects BCD operations by helping identify the previous instruction; The correction differs for addition and subtraction.

Shifting operations can be performed on any register or memory location rather than just on the accumulator. What's more, I/O operations can also be done with any register, rather than just the accumulator. Sixteen-bit direct loads and stores can be sent to the BC-register pair, the DE pair or the IX or IY registers—instead of just the HL as in the 8080. Consequently, the number of exchange and register-move operations is reduced considerably. Also, 16-bit arithmetic operations using the HL pair

## Z80 microprocessor architecture

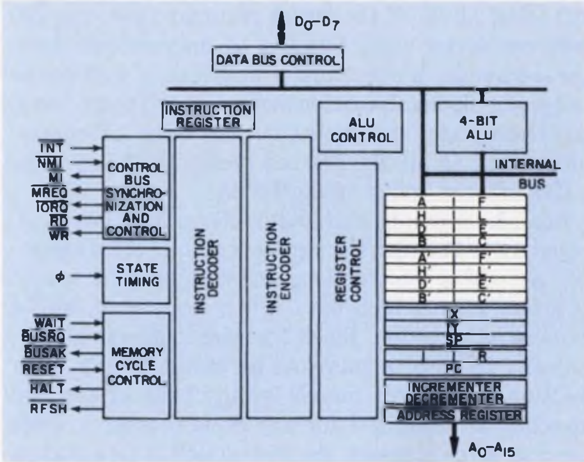
Built into the Z80 microprocessor are all bus-control, memory-control, and timing signals in addition to eight general-purpose 16-bit registers and an arithmetic-and-logic unit (ALU). The Z80 is upward-compatible with the Intel 8080A[1] and 8085 μPs.

All the 8080 registers are duplicated within the Z80 and, in addition to the eight 8-bit registers (A, F, B, C, D, E, H and L) of the 8080, there is an alternate set (A′, F′, B′, C′, D′, E′, H′and L′) and several other special-purpose registers. The additional registers include two 16-bit index registers (IX and IY), an 8-bit interrupt-vector register (I) and an 8-bit memory-refresh register (R). Also carried forward from the 8080 register set are the 16-bit stack pointer and the 16-bit program counter (PC).

Normally, all instructions reference the main register set, and alternate registers are accessed via two exchange commands that swap register contents in the banks. One command, exchanges the accumulator and register flags, while another instruction, exchanges the other six general-purpose registers. Since both instructions are single-byte, minimum-execution-time instructions, a complete swap can be done in four clock cycles (1 μs for a 4-MHz clock). These commands and registers are very handy for rapid single-level interrupt handling.

The Z80's two index registers have no direct corollary in the 8080 architecture, but in operation they resemble the single index register in the 6800 μP.[2] Instructions using this mode such as the accumulator-load command [LD A, (IX + 7)] contain a single-byte offset field (+7, in this case). The effective address of the operand is the sum of the offset and the IX-register contents. This addressing mode is particularly convenient for table references, multibyte entries or for passing a pointer to a group of subroutine parameters. The offset byte is interpreted by the Z80 as a 2's complement number, so both positive and negative indexing is possible.

A special feature of the Z80 is its ability to refresh dynamic memory automatically. Its memory-refresh register acts as a 7-bit counter that is incremented after every op-code fetch. After the fetch, the R-




register contents are loaded onto the low-order seven bits of the address bus, and a status line on the processor goes low to indicate the presence of a valid refresh count. Because this entire process takes place while the op code is decoded internally, it never interferes with any other μP activity on the bus.

The I register forms the high-order eight bits of an address. When an interrupt occurs and the Z80 is in the vectored mode, the lower order eight bits are supplied by an interrupting peripheral. In response to the interrupt, the μP does an Indirect Call instruction with the composite address. All the support chips have corresponding registers that store the low-order eight bits and supply them to the Z80 when the interrupt is acknowledged.

Able to perform 12 basic operations—add, subtract, AND, OR, Ex-OR, compare, test-bit, reset-bit, set-bit, increment, decrement, and left or right-shift and rotate (arithmetic or logic)—the ALU communicates with the registers and external-data bus by means of a buffered internal bus. As each instruction is fetched from memory, it is loaded into the instruction register and decoded by the control section, which supplies all the control signals for the Z80's subsystems.

have been expanded over the 8080's to include add with carry and subtract with borrow.

### Software gives the Z80 horsepower

Many of the instructions available only in the Z80 support the manipulation of multibyte blocks of data —a great plus in data communications and text manipulation. For instance, a block-move instruction takes data from the memory location specified by the HL-register pair, deposits them in the location specified by the DE pair, increments the HL and DE registers and then decrements the BC pair, which is assumed to hold a byte counter for the operation. This instruction can be executed in a single cycle or repeat sequence. Decrementing the HL and DE addresses is also possible.

By using the block move command, the μP can transfer bytes of data at 5.25 μs/byte (for a 4-MHz clock). Block operations are also available for memory searches and I/O operations. And shift and rotate operations have been enhanced. For decimal arithmetic, 4-bit shifts through the accumulator can greatly speed up BCD multiplication and division, and bit-manipulation instructions permit fast access to any bit in either the external memory or an internal register.

Other enhancements of the instruction set include

## Software capabilities of the Z80

Able to execute over 150 different instructions, including all 78 of the 8080A command set, the Z80 features seven basic families of instructions: load-and-exchange, block-transfer-and-search, arithmetic and logic, bit-manipulation (set, reset and test), jump, call-and-return, input/output, and basic μP-control commands. In all, the Z80 can recognize 696 op codes —244 are the codes of the 8080A.

Load instructions move data internally between μP registers or between the registers and external memory. All these instructions must specify a source location, from which data are to be moved, and a destination location. Block-transfer instructions permit any block of memory to be moved to any other location. Search commands let any block of external memory be examined for any 8-bit character. Once the character is found, the instruction is terminated.

The ALU instructions operate on data held in the accumulator and other general-purpose registers or external memory. Results are held in the accumulator, and appropriate flags are set. Bit-manipulation commands allow any bit in the accumulator, any general-purpose register or any external memory location to be set, reset or tested with a single instruction. Jump, Call and Return instructions are used to transfer between various locations in the program.

I/O instructions permit a wide range of transfers between external memory locations or general-purpose Z80 registers and external I/O devices. In either case, the port number is provided on the lower eight bits of the address bus during any I/O operation. Also, the basic μP-control commands include such instructions as setting or resetting the interrupt-enable flip-flop or setting the mode of interrupt response.

In addition to the seven addressing modes of the 8080—direct, register, register indirect, modified page Ø, extended, implied and immediate—the Z80 has three more addressing modes: relative, indexed, and bit addressing—that can be used.

A special byte-call instruction lets the Z80 program proceed to any of eight locations in page Ø of the memory. This modified page Ø addressing allows a single byte to specify a complete 16-bit address, which saves memory space.

Relative addressing lets the Z80 use the byte following the op code to specify a displacement from the current program-counter value. The displacement value is in 2's-complement form, which permits up to a +127 or −128 byte displacement. Extended addressing includes two bytes of address in the instruction.

Index registers can also be used as part of the address. In the indexed addressing mode, a byte of data following the op code is a displacement value that must be added to the specified index register (the op code indicates which register) to form a memory pointer. Also available is an implied addressing mode in which the op code uses the contents of one Z80 register or more as the operands. The last addressing mode lets the Z80 access any memory location or μP register and permits any bit to be set, reset or tested.

| Mnemonic | Description |
|---|---|
| **8-bit load instructions** | |
| LD r, r' | Load register r with r' |
| LD r, n | Load register r with n |
| LD r, (HL) | Load r with location (HL) |
| LD r, (IX+d) | Load r with location (IX+d) |
| LD r, (IY+d) | Load r with location (IY+d) |
| LD (HL), r | Load location HL with r |
| LD (IX+d), r | Load location IX+d from register r |
| LD (IY+d), r | Load location IY+d from register r |
| LD (HL), n | Load location HL with value n |
| LD (IX+d), n | Load location IX+d with n |
| LD (IY+d), n | Load location IY+d with n |
| LD A, (BC) | Load AC with location BC |
| LD A, (DE) | Load AC with location DE |
| LD A, (nn) | Load AC with location nn |
| LD (BC), A | Load location BC with AC |
| LD (DE), A | Load location DE with AC |
| LD (nn), A | Load location nn with AC |
| LD A, I | Load register A from I |
| LD A, R | Load AC with register R |
| LD I, A | Load register I with AC |
| LD R, A | Load register R with AC |
| **16-bit load instructions** | |
| LD dd, nn | Load registers dd with nn |
| LD IX, nn | Load register IX with nn |
| LD IY, nn | Load register IY with nn |
| LD HL, (nn) | Load L with contents of location nn and H with (nn+1) |
| LD dd, (nn) | Load registers dd with location nn |
| LD IX, (nn) | Load IX with location nn |
| LD IY, (nn) | Same but for IY |
| LD (nn), HL | Load location nn with HL |
| LD (nn), dd | Load location (nn) with register pair dd |
| LD (nn), IX | Same but for IX |
| LD (nn), IY | Same but for IY |
| LD SP, HL | Load stack pointer from HL |
| LD SP, IX | Load stack pointer from IX |
| LD SP, IY | Load stack pointer from IY |
| PUSH qq | Load register pair qq onto stack |
| PUSH IX | Load IX onto stack |
| PUSH IY | Load IY onto stack |
| POP qq | Load register pair qq with top of stack |
| POP IX | Load IX with top of stack |
| POP IY | Load IY with top of stack |
| **Exchange, transfer and search instructions** | |
| EX DE, HL | Exchange contents of DE & HL |
| EX AF, A' F' | Exchange contents of AF & A' F' |
| EXX | Exchange all six general purpose registers with alternates |
| EX (SP), HL | Exchange stack pointer contents with HL contents |
| EX (SP), IX | Same but use IX register |
| EX (SP), IY | Same but use IY register |
| LDI | Load (HL) into DE, increment DE and HL, decrement BC |
| LDIR | Same but loop until (BC) = O |
| LDD | Load location (PE) with location (HL) and decrement DE, HL and BC |
| LDDR | Same but loop until (BC) = O |
| CPI | Compare contents of AC with (HL), set Z flat if =, increment HL and decrement BC |
| CPIR | Same but repeat until BC = O |
| CP s | Compare operand s with AC |
| CPD | Same as CPI but decrement HL |
| CPDR | Same as CPIR but decrement HL |
| **8-bit arithmetic and logic instructions** | |
| ADD A, r | Add contents of r to AC |
| ADD A, n | Add byte n to AC |
| ADD A, (HL) | Add contents of HL to AC |

| | |
|---|---|
| ADD A, (IX+d) | Add location (IX+d) to AC |
| ADD A, (IY+d) | Same but (IY+d) |
| ADC A, s | Add with carry operand s to AC |
| SUB s | Subtract contents of r, n, HL, IX+d or IY+d from AC |
| SBC s | Same but also subtract carry flag |
| AND s | Logic AND of operand s and AC |
| OR s | Same but OR with AC |
| XOR s | Same but EX-OR with AC |
| INC r | Increment register r |
| INC (HL) | Increment location (HL) |
| INC (IX+d) | Same but use (IX+d) |
| INC (IY+d) | Same but use (IY+d) |
| DEC m | Decrement operand m |

**16-bit Arithmetic instructions**

| | |
|---|---|
| ADD HL, ss | Add register pair ss to HL |
| ADC HL, ss | Same but include carry flag |
| SBC HL, ss | From HL subtract contents of ss and carry flag |
| ADD IX, pp | Add register pair pp to IX |
| ADD IY, rr | Same but use rr and IY |
| INC ss | Increment register pair ss |
| INC IX | Increment IX register |
| INC IY | Same but IY register |
| DEC ss | Decrement register pair ss |
| DEC IX | Same but IX register |
| DEC IY | Same but IY register |

**General purpose arithmetic & control instructions**

| | |
|---|---|
| DAA | Decimal adjust accumulator |
| CPL | Complement (AC) |
| NEG | Complement (AC) and add 1 |
| CCF | Complement carry flag |
| SCF | Set carry flag = 1 |
| NOP | No operation |
| HALT | Halt, wait for interrupt or reset |
| DI | Disable interrupts |
| EI | Enable interrupts |
| IMØ | Set $\mu$P to interrupt mode Ø |
| IM1 | Set $\mu$P to interrupt mode 1 |
| IM2 | Set $\mu$P to interrupt mode 2 |

**Rotate and shift instructions**

| | |
|---|---|
| RLCA | Rotate AC left |
| RLA | Same but include carry flag |
| RRCA | Rotate AC right |
| RRA | Same but include carry flag |
| RLC r | Rotate register r left |
| RLC (HL) | Rotate location (HL) left |
| RLC (IX+d) | Same but location (IX+d) |
| RLC (IY+d) | Same but location (IY+d) |
| RL m | Same as any RLC but include carry flag |
| RRC m | Same as RLC but shift right |
| RR m | Same as RL m but shift right |
| SLA s | Shift left (any RLC register) |
| SRA s | Same but shift right and keep MSB |
| SRL s | Same as SLA but shift right |
| RLD | Simultaneous 4-bit rotate from $AC_L$ to L, L to H and H to $AC_L$ |
| RRD | Simultaneous 4-bit rotate from $AC_L$ to H, H to L and L to $AC_L$ |

**Bit set, reset and test instructions**

| | |
|---|---|
| BIT b, r | Test bit b of register r |
| BIT b, (HL) | Test bit b of location (HL) |
| BIT b, (IX+d) | Test bit b of location (IX+d) |
| BIT b, (IY+d) | Test bit b of location (IY+d) |
| SET b, r | Set bit b in register r to 1 |
| SET b, (HL) | Same but use contents of location HL |
| SET b, (IX+d) | Same but use contents of location IX+d |
| SET b, (IY+d) | Same but use contents of location IY+d |
| RES b, s | Reset bit b of operand m |

**Jump, c all and return instructions**

| | |
|---|---|
| JP nn | Unconditional jump to location nn |
| JP cc, nn | If condition cc True, do a JP nn otherwise continue |
| JR e | Unconditional jump to PC+e |
| JR C,' e | If C = 0 continue. If C = 1 do JR e |
| JR NC, e | Reverse of JR c, e |
| JR Z, e | If Z = 0 continue. If Z = 1 do JR e |
| JR NZ, e | Reverse of JR Z, e |
| JP (HL) | Load PC from (HL) |
| JP (IX) | Load PC from (IX) |
| JP (IY) | Load PC from (IY) |
| DJNZ, e | Decrement register B and jump relative if B = 0 |
| CALL nn | Unconditional call subroutine at location nn |
| CALL cc, nn | Call subroutine at location nn if condition cc is True |
| RET | Return from subroutine |
| RET cc | If cc false continue, otherwise do RET |
| RETI | Return from interrupt |
| RETN | Return from nonmaskable interrupt |
| RST p | Store PC in stack, load 0 in $PC_H$ and restart vector in $PC_L$ |

**Input/output instructions**

| | |
|---|---|
| IN A, n | Load AC with input from device n |
| IN r, (C) | Load r with input from device C |
| INI | Store contents of location specified by C in address specified by HL, decrement B and increment HL |
| INIR | Same but repeat until B = 0 |
| IND | Same as INI but decrement HL too |
| INDR | Same as INIR but decrement HL too |
| OUT n, A | Load output port (n) with AC |
| OUT (C), r | Load output port (C) with register r |
| OUTI | Load output port (C) with location (HL) and increment HL and decrement B |
| OTIR | Same but repeat until B = 0 |
| OUTD | Same as OUTI but decrement HL |
| OTDR | Same as OTIR but decrement HL |

**Notes**

b represents a 3-bit code that indicates position of the bit to be modified

cc represents a 3-bit code that indicates which of eight condition codes are to be used

d is an 8-bit offset value

dd refers to register pairs BC, DC, HL or the stack pointer

e represents a signed two's complement number between −126 and +129

m is an 8-bit number

n is an 8-bit number

nn refers to two 8-bit bytes

p represents one of eight restart vector locations on page Ø

pp refers to register pairs BC, DE, the IX register or the stack pointer.

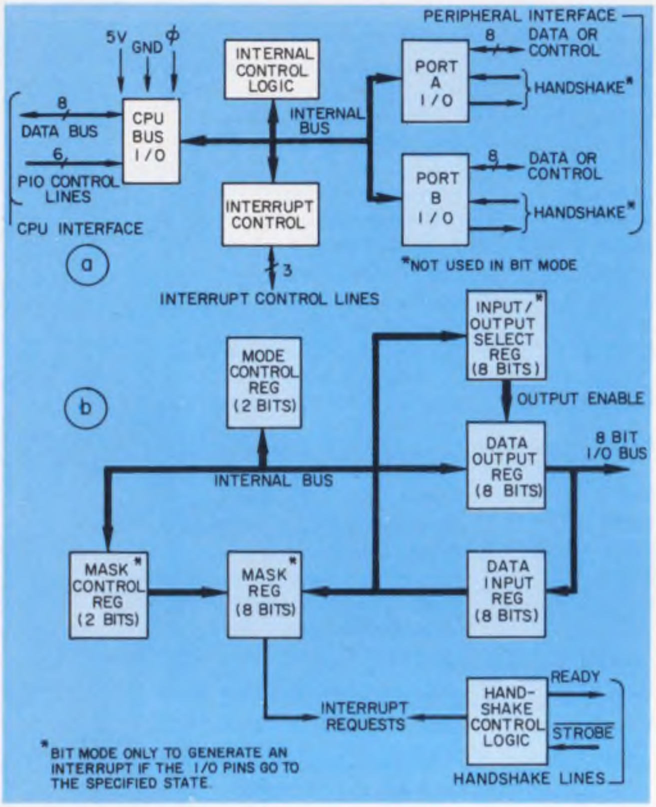
qq refers to register pairs AF, BC, DE or HL

r or r' refers to registers A, B, C, D, E, H or L or their alternates

rr refers to register pairs BC, DE, the IY register or the stack pointer

s refers to either the r registers, the n data word or the contents of locations specified by the contents of the HL, IX+d or IY+d registers

ss refers to register pairs BC, DE, HL or the stack pointer




4. **With two parallel, 8-bit I/O ports,** the PIO circuit (a) can use either of the ports in a parallel system or on a line-by-line basis for 16 separate I/O lines. Inside each port, five control registers are loaded by the Z80 before operation to initialize the port (b).

the decimal-adjust command, which now works after subtract as well as add operations. Negate-instructions and looping commands are also part of the set. The looping instruction decrements the B register and takes a relative branch if that register has not reached zero. Other operations are shown in the box on Z80 software (see page 58).

### Put the Z80 to work

With the four basic Z80 peripheral circuits described virtually any high-performance microcomputer can be constructed. For example, a process-control system can be built around the Z80, as shown in Fig. 3. The peripherals handled by the Z80 controller include three parallel input/output circuits and one counter/timer. The PIOs handle a 16-key keyboard, a printer, a multichannel a/d converter and 16 control lines. Because the peripheral chips can be daisy-chained, a priority interrupt structure can be formed with little or no software or hardware overhead. Using the interrupt mode, the requesting PIO causes the μP to go to a service routine, and, after the routine, a special instruction—return-from-interrupt—goes back to the PIO and allows the μP to service lower-priority interrupts.

All support chips have two lines for daisy-chaining—the Interrupt-enable-in (IEI) and Interrupt-enable-out (IEO). Since a CTC is used in the controller to relieve the Z80 from doing timing loops, software overhead is minimized. For the controller of Fig. 3, 14 ICs are needed—and nine of them are memories (2048 bytes of ROM and 4096 bytes of RAM).

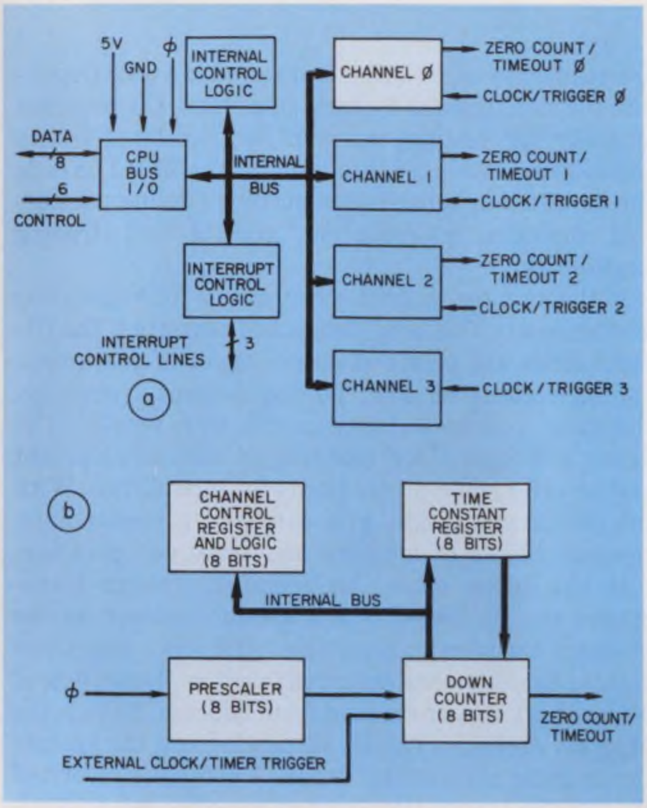
The Z80-PIO, a parallel-interface controller, has two 8-bit ports and provides TTL-compatible interfaces (Fig. 4a). Port A has four possible modes of operation: byte output, byte input, byte bidirectional bus and bit. Port B has all the modes except byte bidirectional. The port I/O logic consists of handshake control and six registers (Fig. 4b): an 8-bit input register, an 8-bit output register, a 2-bit mode-control register, an 8-bit mask register, an 8-bit I/O-select register and a 2-bit mask-control register. The last three are used only when the port is programmed to operate in the bit mode. Of the 40 pins on the PIO, 24 are required by the port and CPU buses, six more for μP interfacing, three for interrupt control, four for handshaking the I/O ports and three for power, ground and the single-phase clock.

Four of the six internal registers are loaded by the Z80 for characteristic programming. The contents of the 2-bit mode-control register determine which of the four PIO operating modes is to be used. Similarly, the 2-bit mask-control register specifies the active state (High or Low) of any peripheral-interface lines which are to be monitored. It also permits an interrupt to be generated when all unmasked pins are active (AND condition) or when any unmasked pin is active (OR condition). The code loaded into the mask register determines which peripheral-device interface pins are to be monitored for the specified status condition. And the code held in the I/O-select register determines which pins are inputs or outputs during bit-mode operation. The other two registers hold incoming or outgoing data.

To relieve some software overhead in timing situations, the CTC provides four channels of programmable timing and counting functions that can be set with software (Fig. 5). Each channel operates in either a timer or counter mode, and programmable interrupts can occur on counter or timer states. Other features include a readable down counter, a selectable 16 or 256 clock prescaler for each timer, a selectable positive or negative trigger for timer initiation and automatic reload of counter or timer constants. In addition three channels have zero count/timeout outputs capable of driving Darlington transistors.

Each channel has two registers, both eight bits long and loaded by the μP. One register, the time-constant register, loads the preset value into the down counter. The other, called a channel-control register, contains the mode and condition information for channel operation. Also included in each channel are an 8-bit down counter and an 8-bit prescaler. The counter is decremented by the prescaler in the timer mode and by the clock-trigger input in the counter mode.

Of the 28 pins on the CTC, eight connect to the data bus, seven to the control lines, three handle interrupt control and three are required for power, ground and




5. **Each CTC provides four channels of counting/timing capability** with an 8-bit counter on each channel (a). There is a control register for each channel and a programmable 8-bit prescaler (b).

the single-phase clock. Three of the four input channels have one input and one output line and the fourth channel has only an input line.

### Speed up data transfer with DMA

One of the interface circuits, a direct-memory-access controller, is designed to effect the high-speed transfer of a block of data between any two ports in a Z80 system and can also be used with other μPs. The circuit is a programmable, single-channel device that provides all address, timing and control signals for the data transfer (Fig. 6). Also, the DMA circuit can search a block of data for a particular, bit-maskable byte, with or without transferring the data. Capable of transfer-only, search-only or search-and-transfer operations at up to 1.2 Mbyte/s, the circuit can automatically increment or decrement the port address from a programmed starting address.

Four communications modes are available on the chip—a byte-at-a-time mode that transfers one byte per request, a burst mode that lets the transfer continue as long as ports are ready, a continuous mode that locks out the μP until the operation is completed, and a transparent mode that steals refresh cycles. When the circuit finds a match or finishes a transfer, it can be programmed to generate an interrupt. Or a complete repeat cycle can be programmed for automatic repeat or repeat on command. A built-in block counter can generate a signal when a certain number of bytes has been transferred—without halting the transfer.

Inside the DMA controller are bus-interface circuits for both the data and address buses, logic and registers to control parameters of the circuit, and address and byte-count circuitry to generate port addresses. There are also provisions for incrementing or decrementing the address, timing circuitry for adjusting the read/write timing of both ports being addressed, and compare logic that permits a byte-matching operation (if a match is encountered, a flag is set in the DMA's status register). Also built-in is the interrupt and $\overline{\text{BUSRQ}}$ logic, which includes a control register that specifies conditions for the chip to generate an interrupt, all the priority-encoding logic to select between generation of an $\overline{\text{INT}}$ or $\overline{\text{BUSRQ}}$ output, and an interrupt-vector register for automatic vectoring to an interrupt-service routine.

Of the 40 pins on the DMA controller, 24 are needed for the address and data bus, and five are needed for the μP control bus. Eight more handle the interrupt control and timing, and three more are necessary for power, ground and clock inputs.

For serial communications, the serial-input/output circuit (SIO) provides two full duplex programmable channels capable of handling asynchronous, synchronous, and synchronous-bit protocols (IBM Bisync, HDLC and SDLC). It can also generate cyclic-redundancy check codes in any synchronous mode. The SIO has four independent serial ports—two for transmitting and two for receiving (Fig. 7). Asynchronous data with 5, 6, 7 or 8 bits and 1, 1-½ or 2-stop bits as well as even, odd or no-parity generation or checking can be handled.

The circuit has × 1, 16, 32 and 64 clock modes and data rates from 0 to 600 kHz. The transmitter sections have eight modem-control lines, quadruple buffers on receiver data and error registers, and double buffers on the transmitter sections. The bus-I/O control block includes the logic for selecting channels and registers, read/write control, and control of special timing for interrupt-acknowledge cycles. Interrupt logic includes the daisy-chain provision as well as two special 8-bit control registers to handle the various interrupt options, as well as an 8-bit vector register for interrupt response.

Three receive buffers allow enough time for interrupt servicing of fast data rates. The receiver-shift register is controlled by the receive-control logic, which includes two 8-bit registers for receive-mode selection and options. There are two more 8-bit registers for programmable-sync characters. The external-status register is an 8-bit, read-only register that indicates the state of the modem-control pins as well as several internal-status conditions. An internal-status register also indicates the state of the SIO. Each channel has its own receive, transmit and status-register banks.

Now that you are familiar with all the basic system-building blocks, you can mold them with software into a working system. Because of the Z80's rich instruction set, assembling software programs by hand can be too complicated for most applications; you should use either a dedicated development system or time-sharing service.

### Development systems speed software

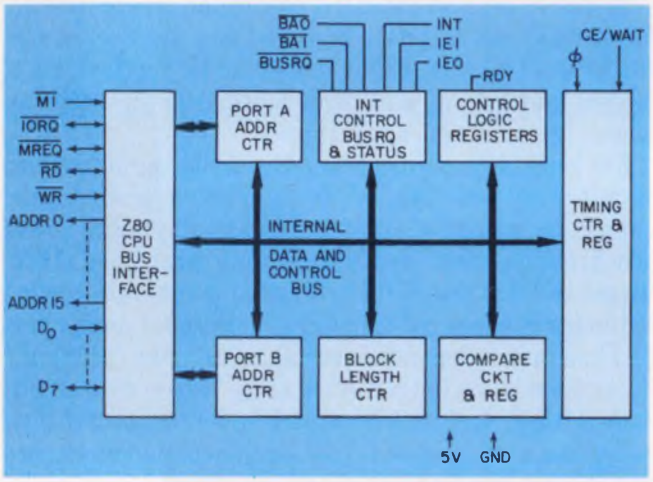
The Z80 development systems and the software available from Zilog include several large dedicated units that permit hardware or software development, or both (Table 2). Also available are assemblers, compilers and time-sharing services as well as Basic and PLZ. (Cobol and Fortran will be available soon.)

All program statements in the development systems are handled by a text editor and stored in a dual floppy-disc file management system. Once filed, the program is ready for testing and can be translated by an assembler or compiler into code for the Z80. The code can be tested by a hardware/software debug package that provides interrogation, control and tracing capabilities.

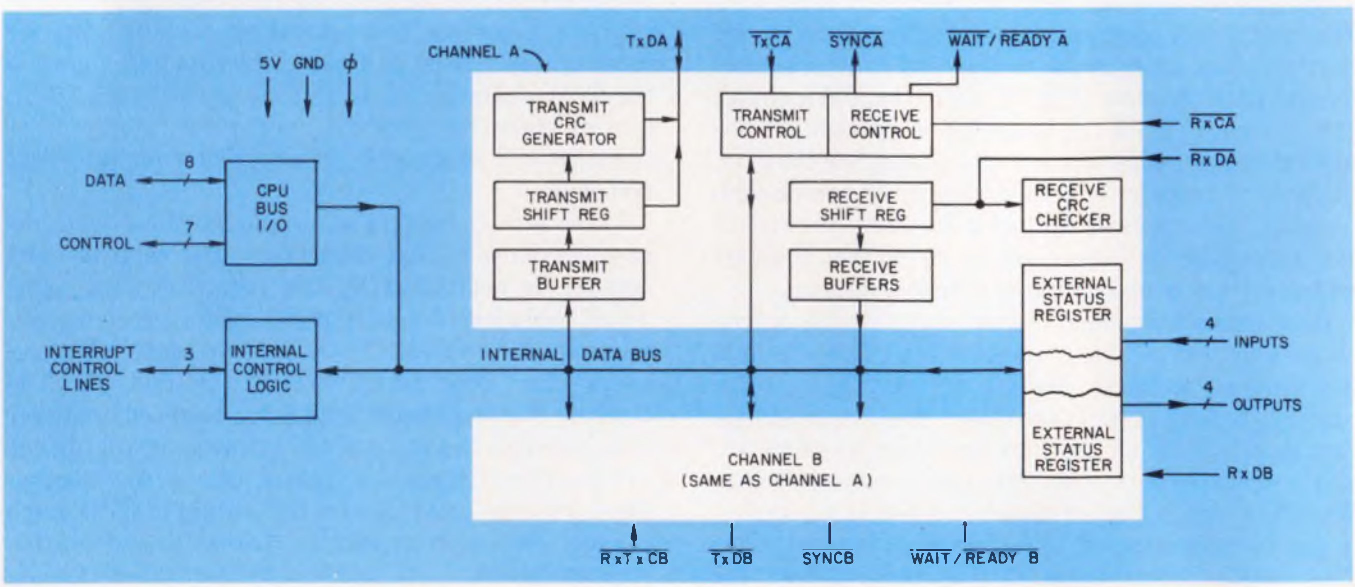
In the monitor mode the system has four operating environments: file, edit, debug and assemble. The file capabilities are pretty standard types of features—storing records on disc, pulling records from disc, changing records and saving the new results. The debug and assembler features of the development system offer some pretty powerful capabilities. With the debug commands, you can set up breakpoints, compare blocks of memory and trace an operation.

In the debug mode, for instance, system transactions can be loaded into a special memory as the program executes in real time. And, once any user-defined condition has occurred (such as the setting of bit 6 of port $8B_{16}$ or reading from address $21C8_{16}$), the program execution can be suspended and the system can re-enter the monitor mode. A complete record of the last 256 transactions just prior to program termination is in the system memory and available to the user.

The main assembler in the development system supports the following features: macros, conditional assembly, the ability to assemble a large file and a sorted-symbol table with cross reference. All these options as well as the printing and listing options are available by setting parameters at the time of assembly. A relocatable assembler with I/O management provides relocatable code and has a linking loader. These permit you also to specify other files that should be included within the current file being




6. **The direct-memory-access controller** has three classes of operation: transfer-only, search-only or search-and-transfer. Any device on the system bus can be controlled by the DMA; internal counters keep track of source and destination addresses.




7. **Two independent full-duplex serial I/O channels** are built into the SIO. Either channel can be programmed to operate in asynchronous or synchronous modes, including BiSync and HDLC/SDLC.

## Table 2. Hardware and software support

| Type | Price unit qty. | Name | Description |
|---|---|---|---|
| Systems | $8990 | Z80-hardware & software development system | 3 kbytes ROM, 1 kbyte RAM for system monitor; 16 kbyte RAM; real-time debug module; dual floppy discs; in-circuit emulator; RS-232 or current loop interface; software and user's manuals; extra card slots; 2 chassis system. Universal interface to printers, PROM programmers, etc. |
| | $6990 | Z80-software development system | Same as above, except no in-circuit emulation capability. |
| | $6990 | Z80-hardware development system | Same as first system, except no universal interface. |
| | $5990 | Z80-microcomputer system | Dual floppy disc system in single chassis containing any combination of Z80 board products (MCB, MDC, etc.) |
| Resident software | N.A. | OSZ80-operating system for Z80 development systems and MCB family | **Assembler:** translates assembly language mnemonics into machine language. Includes macro's, conditional assembly, the ability to assemble programs of virtually any length and sorted symbol tables with complete cross-reference listings. **Relocating assembler and linking loader:** Facility for linking programs which have been assembled independently and executing **Editor environment:** allows the user to input and modify texts, such as, assembly language source programs. **File environment:** controls and manipulates disc files that the user creates while writing, debugging and executing programs. **Debug environment:** allows the user to load, test and save programs using an assortment of debugging aids. |
| | N.A. | BASIC interpreter | This program supports an interpretive language that allows translation into machine code at execution time on a statement-by-statement basis. |
| | N.A. | PLZ-Zilog resident programming language | From relocatable assembly to high-level system programming: • allows access to architecture of Z80 • compiles efficient code • easy to translate to machine language Two levels of the language allow tailoring to programming task needs. |
| Cross software | N.A. | Z80 cross assembler | ANSII 16-Bit Fortran and PLI version available. |
| | | Z80-PLM language compiler | Full PLM language compiler produces Z80 code. |

assembled so you can combine programs.

The text editor in the system includes many commands (for more than many full minicomputer editors) to help you manipulate the source files. Although it is a line editor (the pointer always indicates the beginning of a line), some string-oriented commands are available. Automatic paging permits you to edit files that are larger than available memory work space. Put and Get commands help you copy sections from one disc file to another or insert them into a program. Over 20 commands in the editor permit text repeats, alterations, storage, line-number printing and macro capabilities.

To develop higher-level language programs, you can use a Basic interpreter. This permits programs to be written and debugged interactively. Also made for resident use is PLZ, a procedure-oriented language with a syntactic and semantic style that blends Algol, PL/l and Pascal. It permits access to the Z80 architecture, can compile efficient code and is easy to translate into machine code. Two levels are available: PLZ Level I combines assembly language with statements necessary to create relocatable program modules; Level II is similar to a high-level systems language in which single statements can substitute for sequences of assembly-language statements. ■■

**Acknowledgement**

The circuit designers for the Z80 family were Masatosh Shima (Z80-CPU), Doug Bourn (Z80-PIO), Chuck Glenn (Z80-CTC), Marc Reinig (Z80-DMA) and Ross Freeman (Z80-SIO).

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| Functions & Ranging: | | | |
| dcV | Auto/Manual | Manual | Auto/Manual |
| acV | Auto/Manual | Manual | Auto/Manual |
| dcA | Manual | Manual | Auto/Manual |
| acA | Manual | Manual | Auto/Manual |
| ohms | Auto/Manual | Manual | Auto/Manual |
| Basic Accuracy (dc volts @ 25°C ambient) | ±0.02% reading + 1 digit | ±0.02% reading + 1 digit | ±0.01% reading + 1 digit |
| Full Range Display (Counts) | 19999 | 19999 | 29999 |
| HI/LO Ohms | No | No | Yes |
| Ohms Configuration | 2 terminals | 2 terminals | 2 or 4 terminals |
| Lighted Function Indicator | No | No | Yes |
| Price | $549 | $510 | $525 |

Comparison based on manufacturers' published specifications. Prices are domestic U.S. for ac line-operated instruments.

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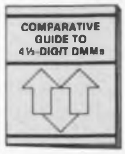


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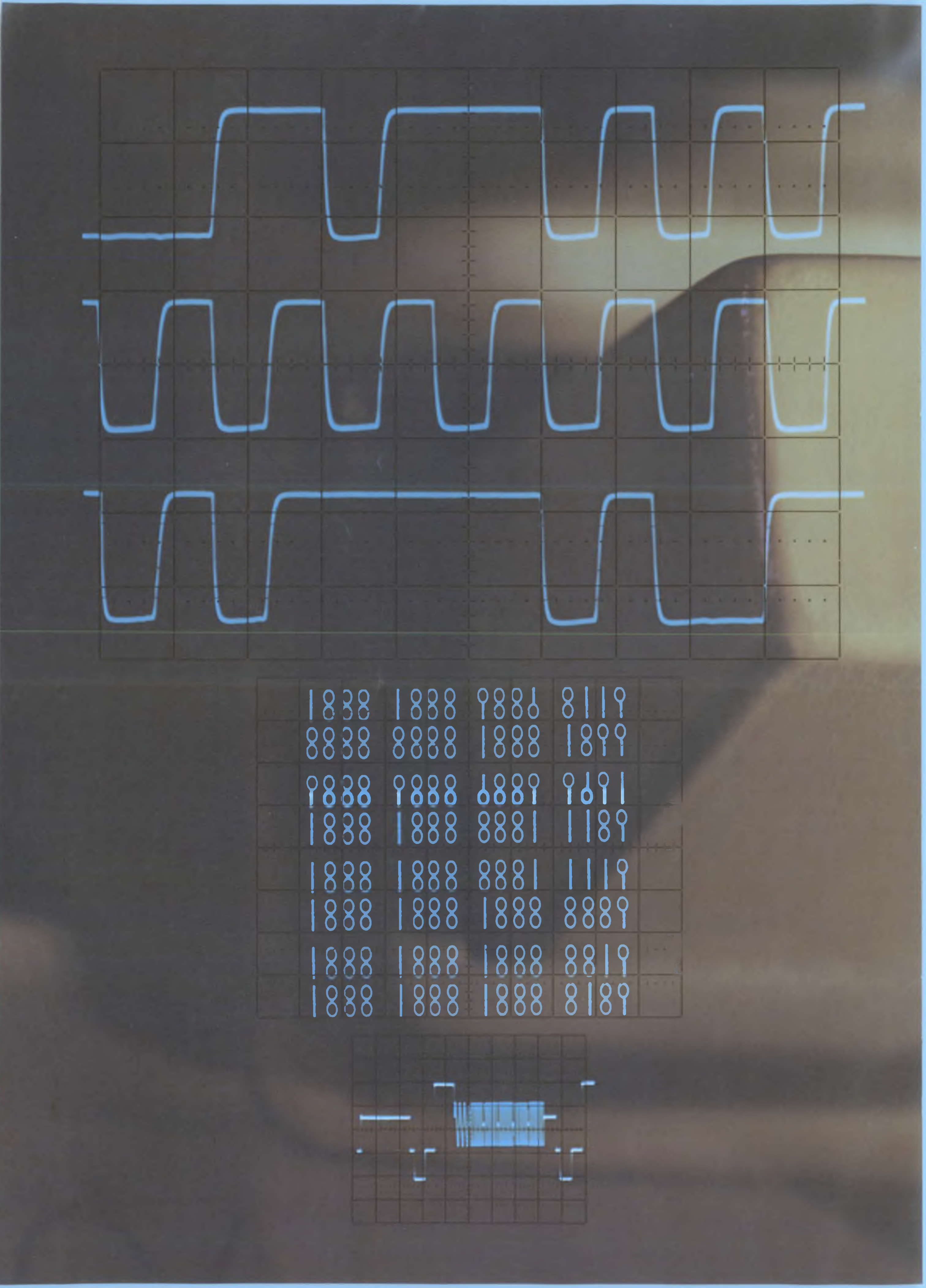
CIRCLE NUMBER 37



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**CIRCLE NUMBER 121**

CIRCLE NUMBER 122

# Dynamic memories offer advantages

## over static RAMs, especially if you need a lot of memory. You can save up to 90% of PC-board space, and money to boot.

Faced with a need to expand memory, you can choose from two basic types: static and dynamic RAM. Because most microprocessors, like the 8080 or 6800, do not provide any control signals or operating modes that would simplify the interface of dynamic RAM to a microprocessor, designers usually prefer static RAM because it's "easier to interface." But before you follow suit, see what dynamic memory has to offer.

Tables 1 and 2 compare the requirements of the two RAM types when used with a Z80 μP. For a 4-k × 8 RAM, there is little difference in power consumption and cost, but the static approach needs 39 chips, while the dynamic alternative requires only 15. The ratio 15/39 = 0.38 is indicated in the "relative size" column.

For the larger memories of Table 2, differences are more pronounced: compared with a 16-k × 8 static RAM, equivalent dynamic memories are vastly superior in power consumption (40% and 21% of static RAM) and size (31% and 10% of static RAM). Even the cost can be much lower (70% with 4-k chips).

Dynamic RAM does have disadvantages—above all the need for a refresh cycle. But if you use a suitable μP, the problems are minor.

The Z80, for instance, is designed to ease interfacing to dynamic RAMs by providing four memory control signals, and a refresh time slot.[1] The signals are memory request, read, write, and refresh.

During the op code fetch cycle, the Z80 also provides a time slot that allows the memory to be refreshed without sacrificing system speed. The refresh cycle is executed during the last two T states of the op code fetch cycle, while the CPU is decoding the op code. During this time period the memory is idle, so that the refresh cycle is "transparent" to the operation of the CPU.

Furthermore, the Z80 provides the refresh row address on address bits $A_0$ to $A_6$ during the fetch cycle. The refresh address is automatically incremented each time a refresh cycle is executed.

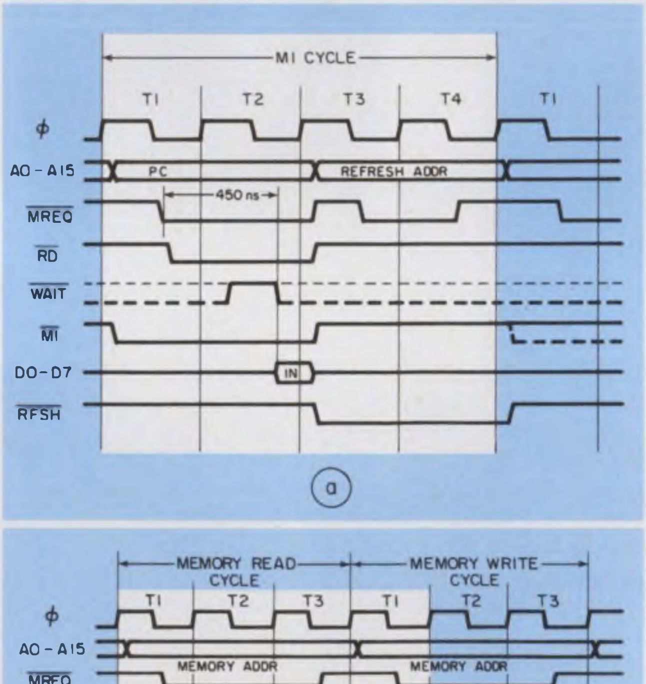
### Timing is the key

Of the Z80's three memory cycles (Fig. 1), the most critical for access time is the op code fetch cycle. Excluding TTL delays, the worst-case access time for the op code fetch is 450 ns (Fig. 1a), while the worst-case access time for the memory-read cycle is 640 ns (Fig. 1b). These access times assume a clock frequency of 2.5 MHz, and are referenced to memory request ($\overline{MREQ}$).

The Z80 microcomputer system puts the extra T-state to good use by placing the refresh cycle in that time slot. No "wait states" or clock "stretching" are required.

To keep track of the row in the memory matrix that is to be refreshed, the Z80 has a dedicated register, R. For the refresh cycle, the Z80 puts the contents of the R register on address lines $A_0$ to $A_6$ and

**Jerry Winfield,** Applications Engineer, Mostek, 1215 W. Crosby Rd., Carrollton, TX 75006




1. **The instruction fetch cycle of the Z80** (a) is longer than the memory read or write cycle (b). The extra time is used to refresh dynamic memories.

automatically increments the R register when an op code fetch is executed. The Z80 memory control signals perform the following functions:

- Memory request ($\overline{MREQ}$) indicates that the address bus holds a valid memory address for a memory-read, or memory-write.
- Read ($\overline{RD}$) indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory uses this signal to gate data onto the CPU data bus.
- Write ($\overline{WR}$) indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
- Refresh ($\overline{RFSH}$) indicates that the lower seven bits of the address bus contain a refresh address for dynamic memories. The current $\overline{MREQ}$ signal is used to refresh all dynamic RAMs in the system.

Mostek's MK4027 (4 k × 1) and MK4116 (16 k × 1) 16-pin dynamic memories use a special address multiplexing technique that loads the address bits into memory and allows each memory to be packaged in a 16-pin DIP. The MK4027 needs 12 address bits to select one out of 4096 locations, and the MK4116 requires 14 bits to select one out of 16,384.

### Refresh your 16-pin RAM

The internal memory can be thought of as a matrix: The MK4027 matrix is 64 × 64, while the MK4116 matrix is 128 × 128. To select a particular location, a row and column address is supplied to the memory. For the MK4027, address bits $A_0$ to $A_5$ form the row address and bits $A_6$ to $A_{11}$ the column address. For the MK4116, address bits $A_0$ to $A_6$ form the row

## Table 1. Comparison of 4-k × 8 static and dynamic RAMs

| Device used | Number of RAMs | Support ICs | Voltages, currents | Over-all power[1] | Relative power | Relative cost[2] | Relative size |
|---|---|---|---|---|---|---|---|
| 21L02 1 k × 1 static | 32 | 7 | +5 V @ 1.26 A | 6.3 W | 1 | 1 | 1 |
| MK4027-4 4 k × 1 dynamic | 8 | 7 | +5 V @ 0.42 A<br>+12 V @ 0.25 A<br>−5 @ 0.03 A | 5.25 W | 0.83 | 0.90 | 0.38 |

## Table 2. Comparison of 16-k × 8 static and dynamic RAMs

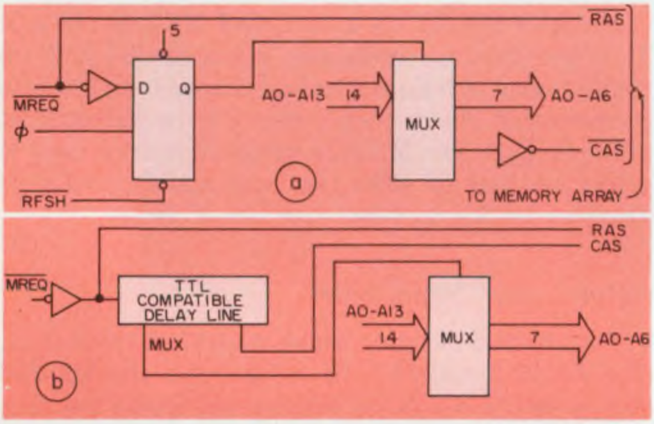
| Device used | Number of RAMs | Support ICs | Voltages, currents | Over-all power[1] | Relative power | Relative cost[2] | Relative size |
|---|---|---|---|---|---|---|---|
| 21L02 1 k × 1 static | 128 | 28 | +5 V @ 5.04 A | 25.2 W | 1 | 1 | 1 |
| MK4027-4 4 k × 1 dynamic | 32 | 16 | +5 V @ 0.55 A<br>+12 V @ 0.60 A<br>−5 V @ 0.03 A | 10.1 W | 0.40 | 0.7 | 0.31 |
| MK4116-4 16 k × 1 dynamic | 8 | 8 | +5 V @ 0.42 A<br>+12 V @ 0.25 A<br>−5 V @ 0.03 A | 5.25 W | 0.21 | 1.08 | 0.10 |

Notes (1) Power requirement of dynamic RAMs is based on Z80 operating at 2.5-MHz clock frequency.
(2) Relative cost includes RAMs, support ICs, power supply, and PC board.

address and bits $A_7$ to $A_{13}$ the column address.

Both the row and column addresses are strobed into the memory by negative-going signals, one called row-address strobe ($\overline{RAS}$), the other a column-address strobe ($\overline{CAS}$). They latch the address bits into the memory for access to the desired memory location.

To retain valid data, the MK4027 needs 64 refresh cycles every 2 ms, while the MK4116 needs 128 refresh cycles every 2 ms, due to its larger memory matrix. In other words, an MK4027 has to be refreshed every 32 µs, while the MK4116 needs refreshing every 16 µs. The memory is refreshed each time a read or write cycle is performed, or by a $\overline{RAS}$-only refresh cycle. (For detailed information on the MK4027 and the MK4116, write for the manufacturer's literature.[2])



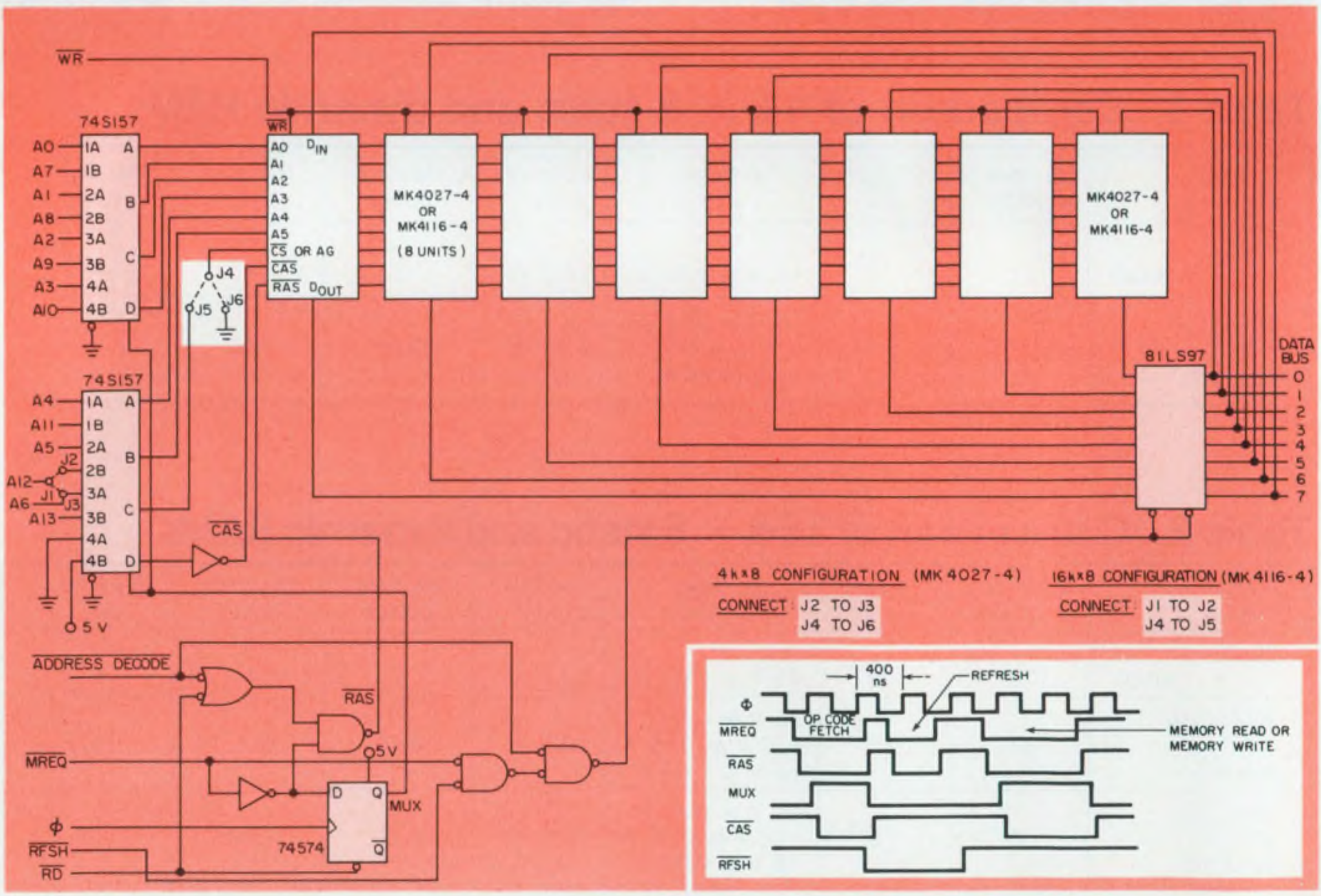

2. **Memory timing signals** can be generated differently for small (a) or large (b) memory arrays.

### The Z80 needs some help

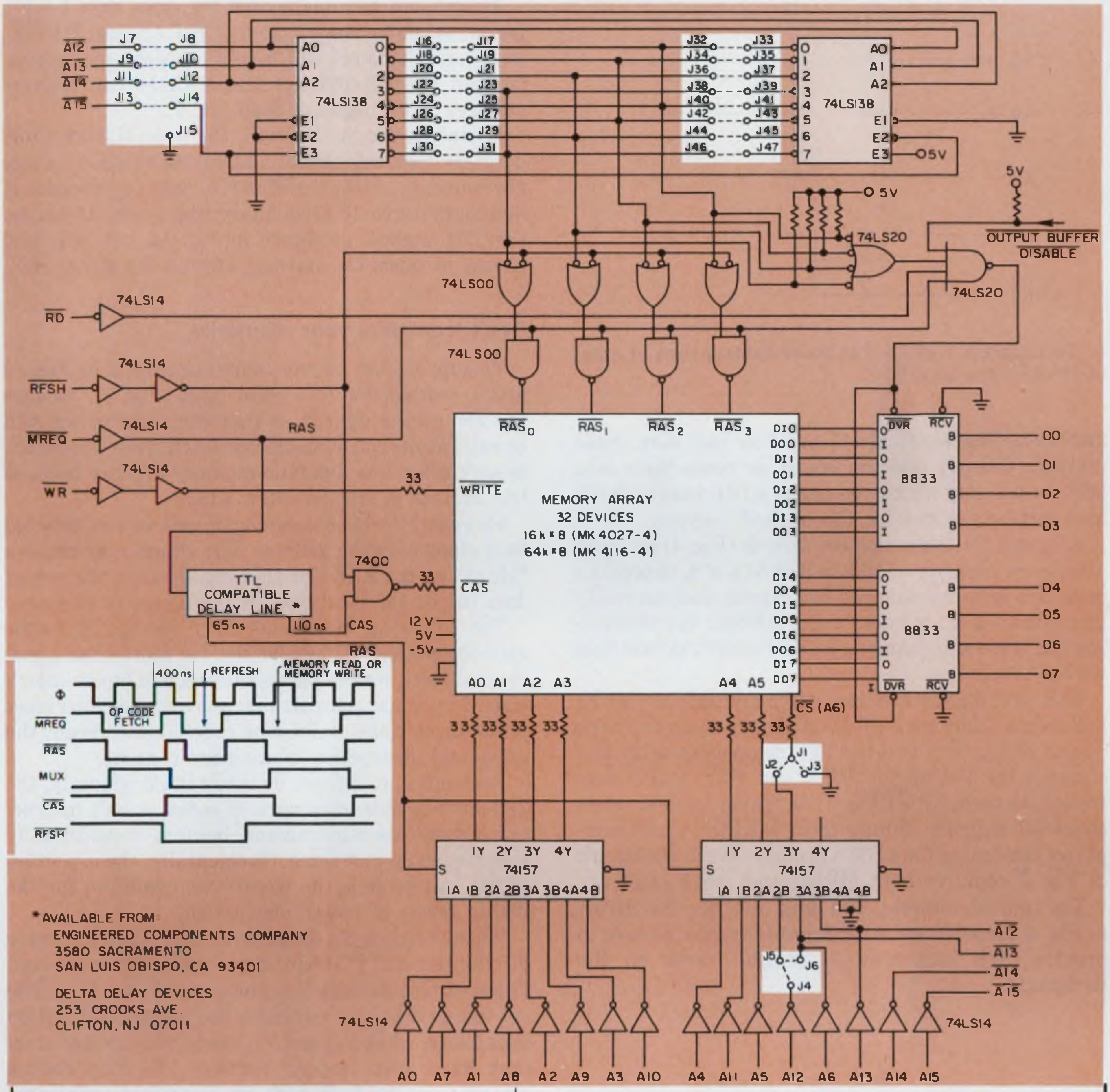
When interfacing a Z80 to a 16-pin dynamic RAM, two timing signals not generated by the Z80 are necessary: the switch multiplexer (MUX) and the column address strobe ($\overline{CAS}$). You can provide them in several ways: Fig. 2a shows a circuit that's best suited for a small on-board memory, while Fig. 2b shows one that suits a separate memory board.

The complete schematic for a small "on-board" memory (Fig. 3) can accommodate either the MK4027-4 or the MK4116-4. Control signal $\overline{MREQ}$ is gated with $\overline{AD}$ (address decode) or $\overline{RFSH}$ to generate $\overline{RAS}$, while $\overline{MREQ}$ and Φ generate MUX. The column address strobe $\overline{CAS}$ is then generated by an output of one of the 74S157 multiplexers.

This design can easily be expanded from a 4-k × 8 memory to a 16-k × 8, by changing two jumpers




3. **The schematic for a 4-k × 8 memory** makes provisions for expansion to 16-k × 8 bits.




**16-k × 8 CONFIGURATION (MK 4027)**

CONNECT: J1 to J3, J5 to J6, J7 to J8, J9 to J10, J11 to J12, J13 to J14

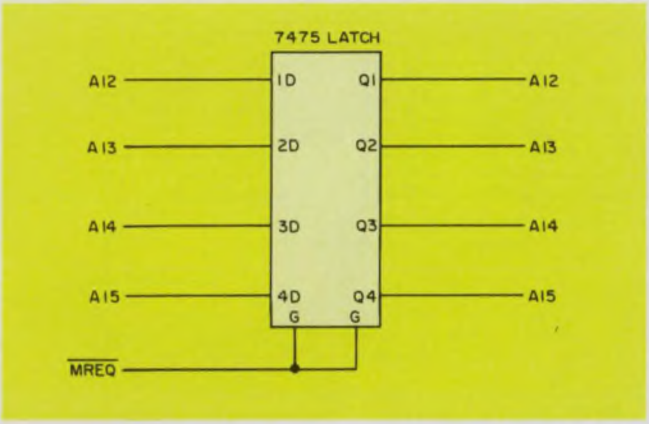
- ADDRESS: 0-3FFF — CONNECT: J24 to J25, J26 to J27, J28 to J29, J30 to J31
- ADDRESS: 4000-7FFF — CONNECT: J16 to J17, J18 to J19, J20 to J21, J22 to J23
- ADDRESS: 8000-BFFF — CONNECT: J40 to J41, J42 to J43, J44 to J45, J46 to J47
- ADDRESS: C000-FFFF — CONNECT: J32 to J33, J34 to J35, J36 to J37, J38 to J39

**64-k × 8 CONFIGURATION (MK 4116)**

CONNECT: J1 to J2, J4 to J5, J8 to J11, J10 to J13, J12 to J15, J14 to J15

ADDRESS: 0-FFFF — CONNECT: J32 to J33, J34 to J35, J36 to J37, J38 to J39

4. **A large dynamic RAM-board** can also be expanded with a special jumper-DIP (white).



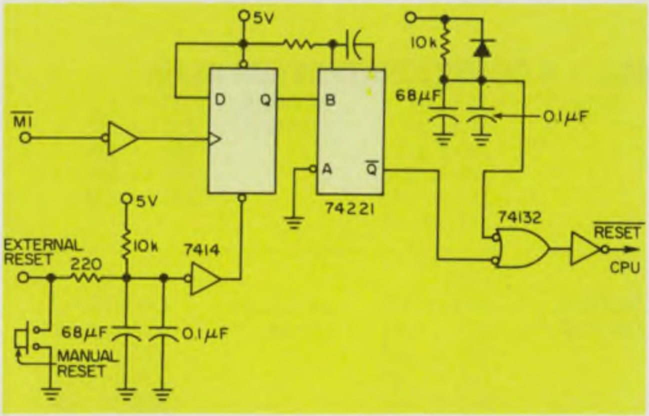

5. **To suppress a glitch that could destroy rows of data,** use this simple quad latch.

and installing eight MK4116s. You can wire these jumpers directly into the board, or route them to a DIP socket, into which you insert a DIP header that's appropriately wired for the desired memory.

A circuit for large memory boards (Fig. 4) provides a memory capacity of 16 k × 8 or 64 k × 8, depending on which memory chip you use. Again, you can easily upgrade a 4-k × 1 memory using MK4027 by substituting MK4116s and changing a DIP header that has prewired jumpers.

This circuit generates the switch multiplexer (MUX) and column-address strobe ($\overline{CAS}$) differently from the circuit in Fig. 3. A two-tap TTL-compatible delay line controls the timing for MUX and $\overline{CAS}$ and is controlled, in turn, by $\overline{MREQ}$. This timing method references all memory timing from $\overline{MREQ}$—which simplifies the timing for a DMA system—while the circuit of Fig. 3 requires both $\overline{MREQ}$ and the $\Phi$ clock.

The control, address, and data lines for the circuit in Fig. 4 are buffered with Schmitt-trigger devices to provide high immunity to possible noise on the backplane.




6. **This auxiliary circuit** limits the length of reset signals to prevent memory loss.

You should terminate memory lines that have a heavy capacitive load ($A_0$ to $A_5$, $\overline{CS}$, $\overline{CAS}$, and $\overline{WRITE}$) with series resistors which help suppress undershoot. Neither the MK4027 nor the MK4116 can tolerate voltages more negative than −1 V.

When you use the MK4027, the two 74LS138 3-to-8 decoders together permit addressing to start on any 4-k boundary. With the MK4116, only one decoder is necessary to give 16-k-boundary addressing. If you use two DIP sockets as shown in Fig. 4a, you will find it easy to select the starting address for either chip.

### Don't jeopardize your memories

To support the memory circuits shown in Figs. 3 and 4, you need a 7475 quad latch (Fig. 5), because the Z80 cannot guarantee that the address bus will be valid at the end of an op code fetch cycle. This quirk doesn't affect the dynamic memory directly because the address is latched internally.

However, the $\overline{RAS}$ decoding circuit will be affected by a change on the address bus, which may cause a "glitch" on the $\overline{RAS}$ line that can destroy one row of data (64 or 128 locations) in the dynamic memory.

The following conditions may destroy dynamic memory content if they persist for more than 1 ms: manual reset, wait-state operations, and bus acknowledge. So you use a circuit that generates a short reset pulse, three clock cycles long (Fig. 5), to prevent the accidental destruction of memory content.

Remember, to refresh dynamic RAM properly, the Z80 must be able to execute op codes. A halt instruction meets this requirement, because it continually executes an op code fetch. (Incidentally, the execution of the halt cycle is the worst-case condition for the Z80 in terms of power dissipation.)

When you design a dynamic memory, proper power distribution and PC-board layout are very important. Power-supply voltage $V_{DD}$ and ground should be laid out in a grid to help minimize the power-distribution impedance, while $V_{BB}$ and $V_{CC}$ needn't be gridded since they have lower supply currents. To help reduce system noise, a 0.1 μF, high-quality ceramic capacitor is recommended on both $V_{CC}$ and $V_{BB}$ for each device, and one 0.1 μF on $V_{CC}$ for each row of eight RAMs.

Lines such as $A_0$ to $A_5$, $\overline{CS}$, $\overline{CAS}$, and $\overline{WRITE}$ are best bused together as rows. Then all the rows can be bused together at one end of the array. Avoid interconnecting these rows. Lines carrying $\overline{RAS}$ are bused together as a row and then connected to the appropriate $\overline{RAS}$ driver. The layout for a 32-device array can be put in a 5 × 5 in. space on a two-sided PC board.■■

**References**

1. *Z80 CPU Technical Manual,* Mostek Corp., 1215 W. Crosby Rd., Carrolton, TX 76005.

2. *Mostek Memory Products Catalogue,* Mostek Corp.

# The 8080 "Ice Breaker"

## Portable for
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| BREAKTHROUGH QUESTIONS | muPro-80E | INTEL® MDS + ICE* |
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| Low cost In-Circuit Emulator? | **YES**, (no terminal req'd) $3,250. | **NO**, $5,400. plus terminal cost |
| Real time execution from emulator or users system memory? | **YES**, phase locked to user clock; rate up to 2.86 mHz | **NO**, emulator resident programs execute slower than real time |
| Memory available to user in 16K emulator system? | **ALL 16K** | **LESS THAN 4K** (12K+used by ICE-80 driver) |
| Totally transparent control/display functions? | **YES** | **NO**, imposes memory, I/O and interrupt restrictions |
| High-level relocatable language supported by 16K paper tape or 32K disk system? | **YES**, BSAL-80 | **NO**, PL/M® requires 64K disk system |
| Assembly language efficiency with high level language? | **YES**, BSAL-80 | **NO**, PL/M® burdened with typical compiler inefficiences |
| Multi-user/Multi-task disk operating system? | **YES**, plus concurrent batch capability | **NO**, single user/single task |
| Portable for development, test, and field service? | **YES**, 4.6" x 6.6" x 15" 18 lbs. | **NO**, 8.5" x 19" x 17" 65 lbs. Plus terminal |

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RECORD MODE
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# **Use microprogram control** on your analog tester and expand capabilities at the 'drop' of a PROM. The unit grades products, too.

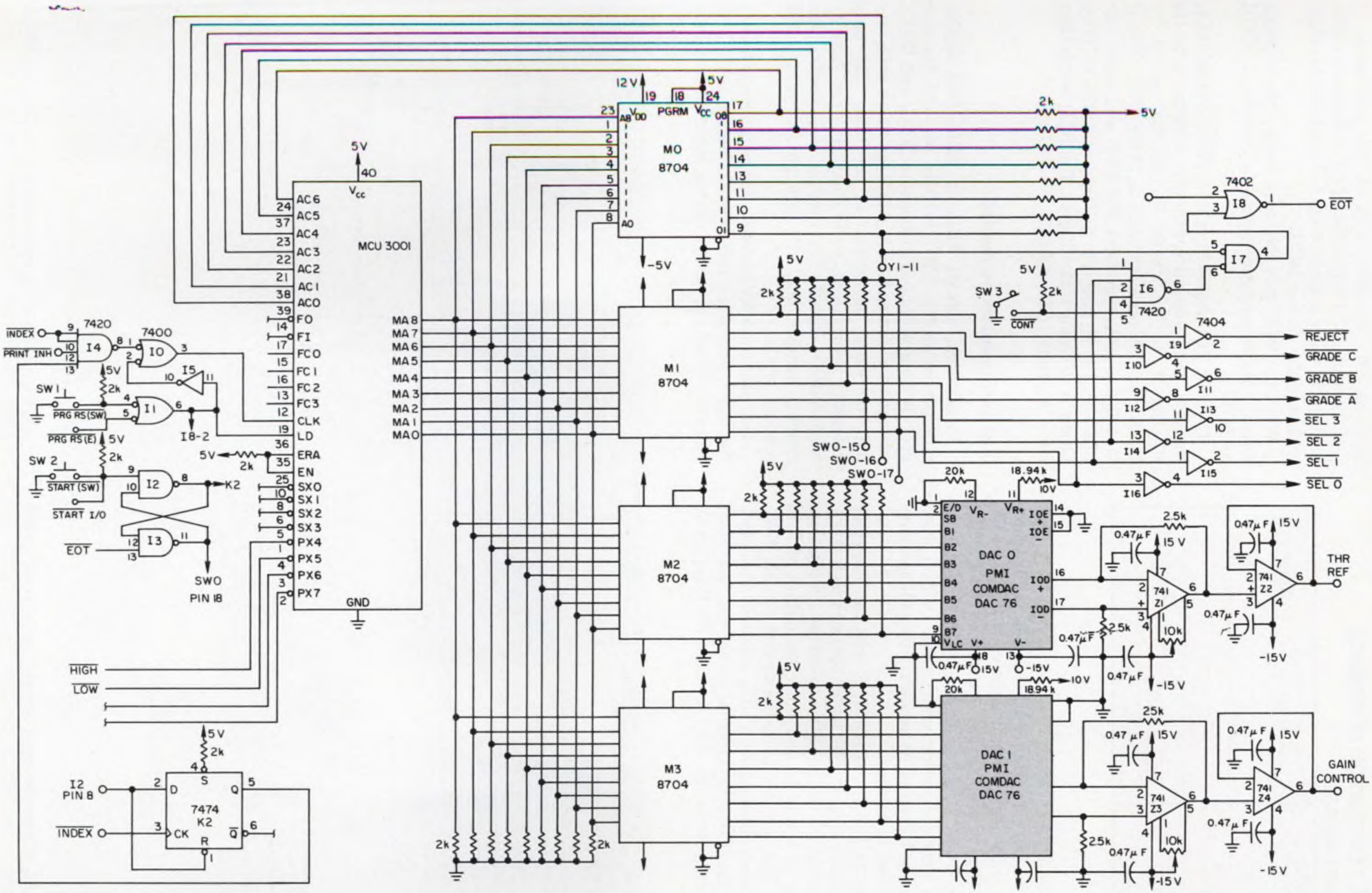
You can design a microprogrammable analog tester that pinpoints device failures by varying the device's threshold voltage. The tester can handle many devices or measure several parameters on any one device. And it can grade product quality.

**N.N. Patel,** Senior Electronic Design Engineer, Control Data Corp., 11615 "I" St., Omaha, NE 68137.

Measurements include temperature, pressure, vibration or surface flatness (as measured by differential transducers); or, the tester can check out a magnetic memory. The firmware program is expand-

## Table 1. Microcoding format for 3001 control unit

| | $AC_6$ | $AC_5$ | $AC_4$ | $AC_3$ | $AC_2$ | $AC_1$ | $AC_Ø$ | $MA_8$ | $MA_7$ | $MA_6$ | $MA_5$ | $MA_4$ | $MA_3$ | $MA_2$ | $MA_1$ | $MA_Ø$ | Memory address in hex | Micromemory output in hex $MØ_Ø$ | $MØ_1$ | $MØ_2$ | $MØ_3$ | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ØØØ | F2 | ØØ | | | Ready to test CH Ø |
| JPX | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | Ø11 | F4 | ØØ | | | "HIGH" detected |
| JPX | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Ø21 | F6 | ØØ | | | "HIGH" detected |
| JPX | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | Ø12 | F4 | ØØ | | | "LOW" detected |
| JPX | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | Ø22 | F6 | ØØ | | | "LOW" detected |
| JPX | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | Ø31 | Ø9 | 8Ø | | | Reject CH Ø because of HIGH |
| JPX | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | Ø32 | Ø9 | 8Ø | | | Reject CH 1 because of LOW |
| JPX | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Ø1Ø | Ø9 | 1Ø | | | CH Ø Grade A |
| JPX | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Ø2Ø | Ø9 | 2Ø | | | CH Ø Grade B |
| JPX | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Ø3Ø | Ø9 | 4Ø | | | CH Ø Grade C |
| JPC | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Ø4Ø | F2 | Ø1 | | | Start CH 1 |
| JPC | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1CØ | F2 | Ø7 | | | Start CH 7 |
| JPX | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1D1 | F4 | Ø7 | | | "HIGH" detected |
| JPX | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1E1 | F6 | Ø7 | | | "HIGH" detected |
| JPX | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1D2 | F4 | Ø7 | | | "LOW" detected |
| JPX | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1E2 | F6 | Ø7 | | | "LOW" detected |
| JPX | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1F1 | ØØ | 87 | | | Reject CH 7 because of HIGH |
| JPX | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1F2 | ØØ | 87 | | | Reject CH 7 because of LOW |
| JPX | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1DØ | ØØ | 17 | | | CH 7 Grade A |
| JPX | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1EØ | ØØ | 27 | | | CH 7 Grade B |
| JPX | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1FØ | ØØ | 47 | | | CH 7 Grade C |




**1. This microprogrammable analog-signal tester** holds test sequences in PROM (8704) and is controlled by a microprogram control unit (3001). The DAC76 d/a converters produce bipolar reference voltages for comparison with the input signals. Outputs include a Reject and a Grading signal.

## Table 2. Formation of grading and reject signals

| High detected | Low detected | Grade |
|---|---|---|
| Once | - - - - | B |
| - - - - | Once | |
| Twice | - - - - | C |
| - - - - | Twice | |
| Three times | - - - - | Reject |
| - - - - | Three times | |
| None | None | A |

able up to 32 channels.

A special d/a converter (PMI DAC 76) in the tester provides both negative and positive threshold voltages. An Intel microprogram control unit (3001 MCU) plus four 8704 PROMs generate both test sequences and 8-bit data for the converter (Fig. 1). And word length can be increased as necessary by adding microprogrammed memories.

The design is self-contained, or you can interface it to a microprocessor. The tester operates as follows:

Press the start switch ($SW_2$) to set the RS flip-flop, consisting of $I_2$ and $I_3$, and cause the output of $I_2$ to go high. This enables both the analog switch, $SW_1$, and the index pulse through $I_4/I_0$, and delivers a clock pulse to the 3001. An external signal can also start things going. Start the 3001 and the RS flip-flop by pressing $SW_1$, or again, with an external signal.

At the end of the first index, flip-flop $K_2$ is set, which enables the index pulse through $I_4/I_0$ and thus provides a clock pulse to the MCU.

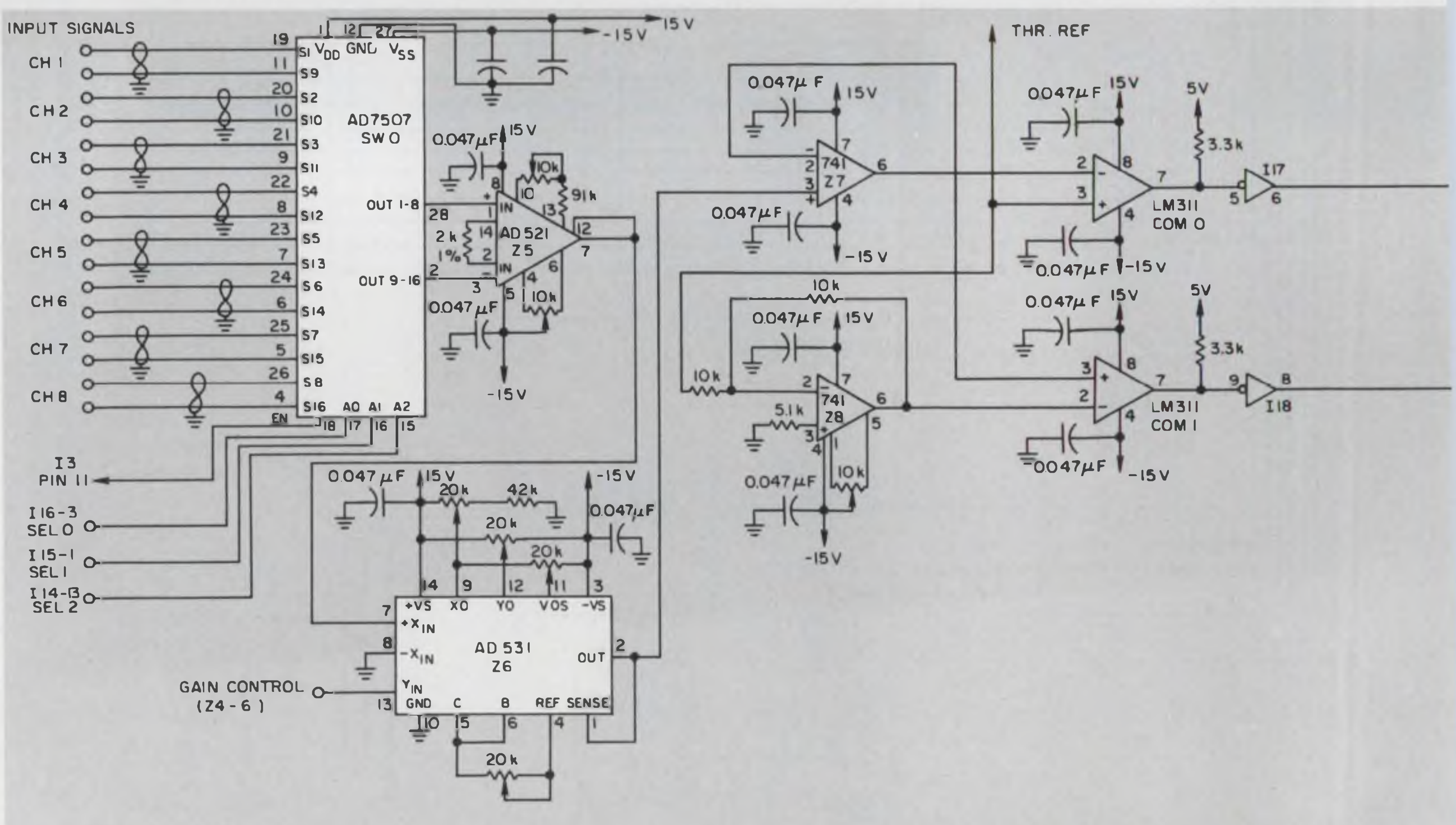
When the MCU gets the index pulse, the detecting circuit has one sequence period to generate a HIGH or LOW.

The 3001 MCU starts from state 000H. Outputs $MA_0$ through $MA_8$ are micromemory address bits for PROMs $M_0$ to $M_3$. PROM $M_0$ outputs, except $O_1$, provide next states $A_0$ through $A_6$ to the MCU. Output $O_1$ acts as a print command. The lower and upper four bits of PROM $M_1$ generate BCD outputs $SEL_0$ to $SEL_3$, Grade A to Grade C and Reject. The BCD words then drive a printer (HP 5055A).

### Just two instructions needed

In addition, signals $SEL_0$ to $SEL_2$ feed analog multiplexer switch $SW_1$. PROMs $M_2$ and $M_3$ also provide binary data to converters $DAC_0$ and $DAC_1$, respectively. Coding for PROMs $M_2$ and $M_3$ is arbitrary and, therefore, not shown in the table. The only necessary instructions are JPX and JPC (see Table 1). Next-address inputs $AC_4$ through $AC_2$ control the channel number, and $AC_1$ through $AC_0$ control the product grade.

Text sequences for channels 1 through 8 start when the index pulses are received. Converter $DAC_0$ provides the threshold voltage during each test sequence,



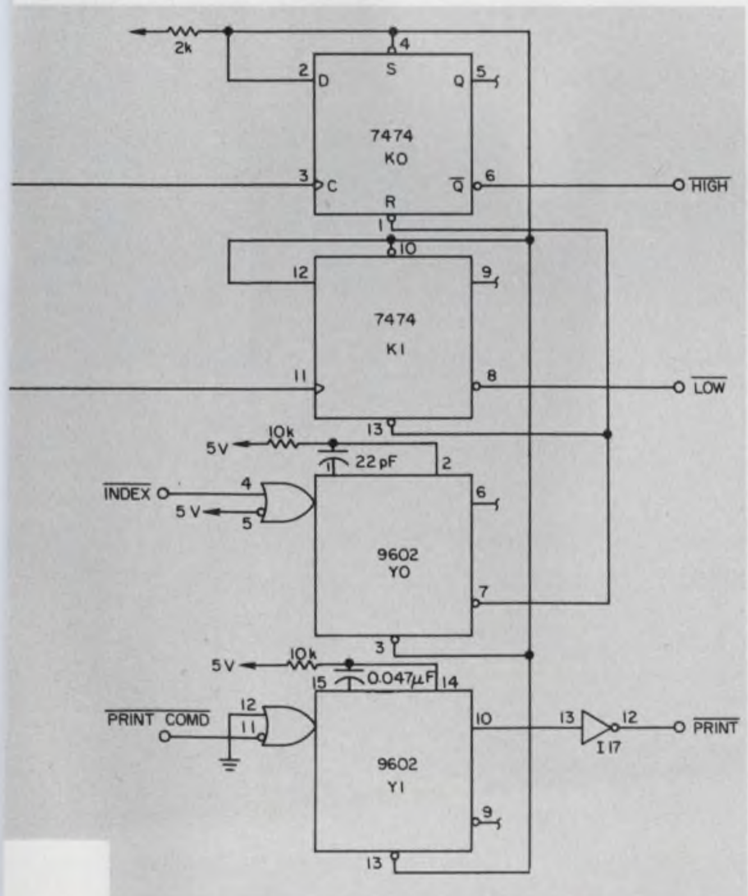

2. **Up to 32 differential-input signals can be multiplexed** in the tester. The LM311s compare the reference and processed input signals and provide the $\overline{HIGH}$ or $\overline{LOW}$ to increase or decrease the threshold level.

and $DAC_1$ controls the gain of the AD531 amplifier. The variable gain is programmed by $M_3$ so that instrumentation amplifier $Z_6$ provides 5 V pk-pk for a differential sinusoidal signal or 5 V dc for a differential dc voltage during any test sequence (Fig. 2).

The analog-multiplexer switch $SW_0$ handles the input differential voltages on channels 0 to 7. The outputs of $SW_0$ connect to instrumentation amplifier $Z_5$, while op amp $Z_7$ acts as a buffer. At the end of testing on channel 7, gate $I_7$ goes high, since $M_0(01)$ is high, and EOT clears the RS flip-flop comprised of $I_2$ and $I_3$. A new test sequence is started by pressing PRG RS (SW), then START (SW). Switch $SW_3$ inhibits the EOT signal, and the program continues from channel 0 through 7, and back.

During the test sequence, if the parameter voltage increases or decreases with respect to the threshold voltage, one of two comparators, $COM_0$ or $COM_1$, fires. The one that fires sets either flip-flop $K_0$ or $K_1$. This setting generates a HIGH or LOW signal that directs the MCU 3001 to continue the test sequence on the same channel and to decrease or increase the threshold voltage.

PROM $M_2$ generates the Product Grade (A to C) and Reject signals (Table 2). Note that flip-flops $K_0$ and $K_1$ are cleared at the start of a test sequence. If no error is detected (neither a HIGH nor LOW), the PRINT COMD comes on and triggers the single shot, $Y_1$. The HP 5055 then prints the channel number and grade in hex code. ■■



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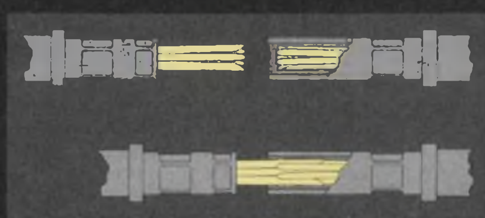

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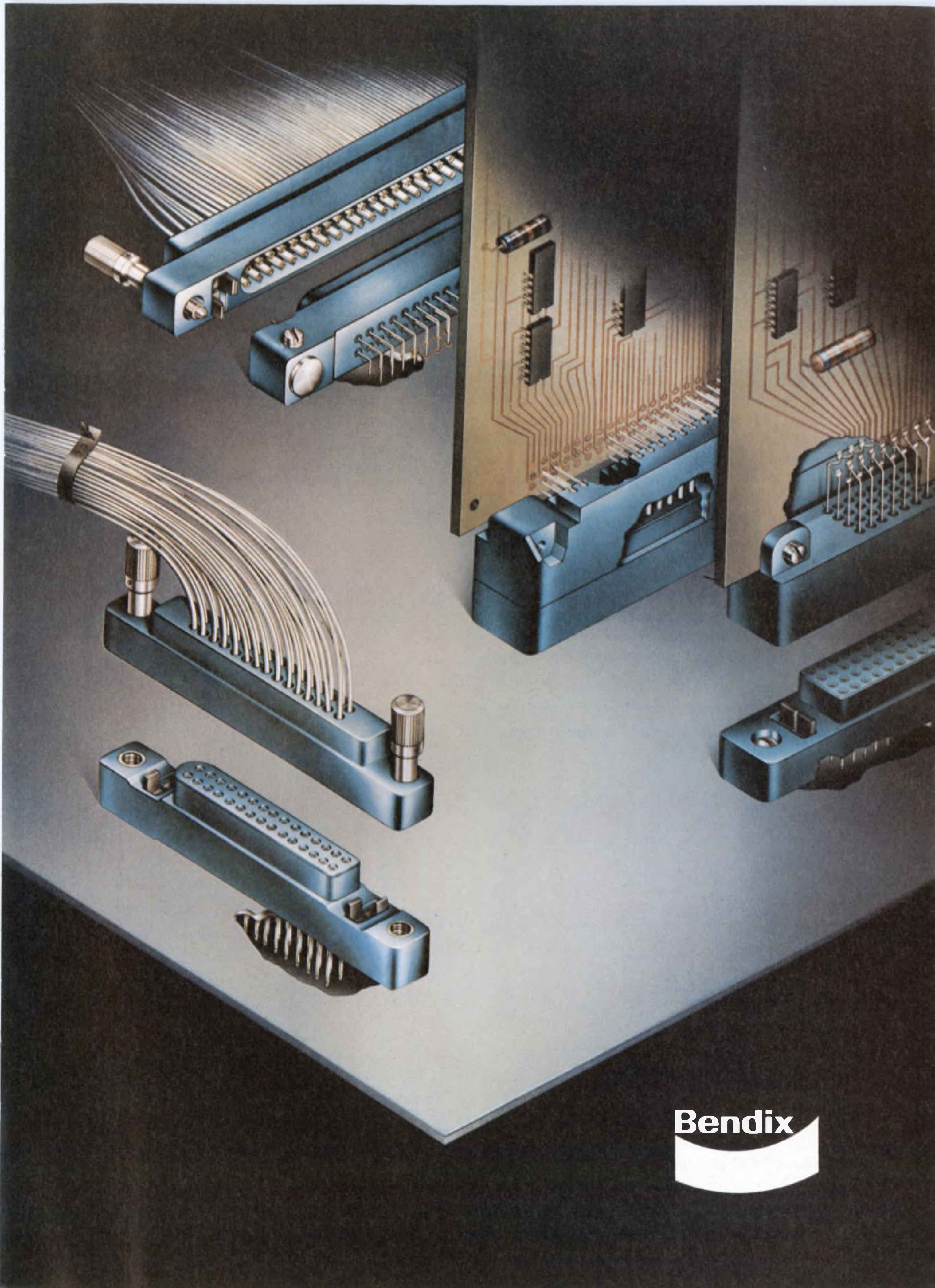
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# Select a character/function decoder

## that optimizes cost, board space and wiring. Hardware or firmware? The number of codes determines the best method.

It's easy to say, "Save time, board space and money by selecting the proper function-and-character decoder for your logic system." But the many available decoding methods—with their frequently overlapping advantages and disadvantages—make selection frustrating. Not only must you consider the usual hardwired methods, but you must also include firmware decoders that can be modified by program changes.

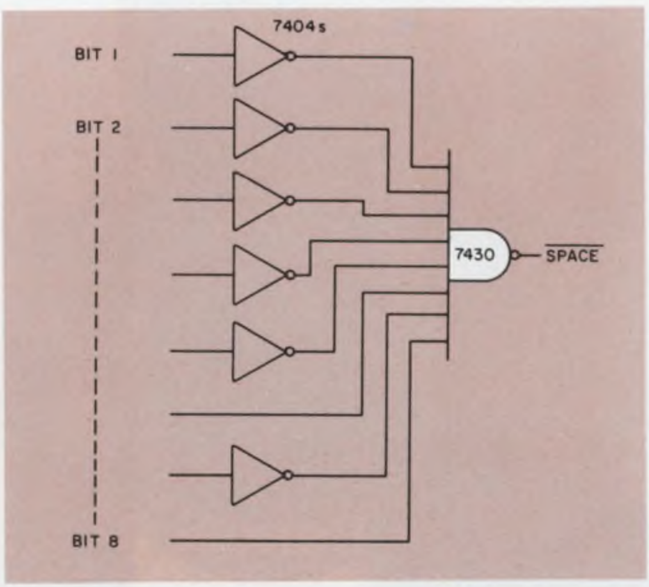
Nevertheless, studying the decoder methods to be described will give you a firm basis for making rational, clearcut choices.

### Which decoder is best?

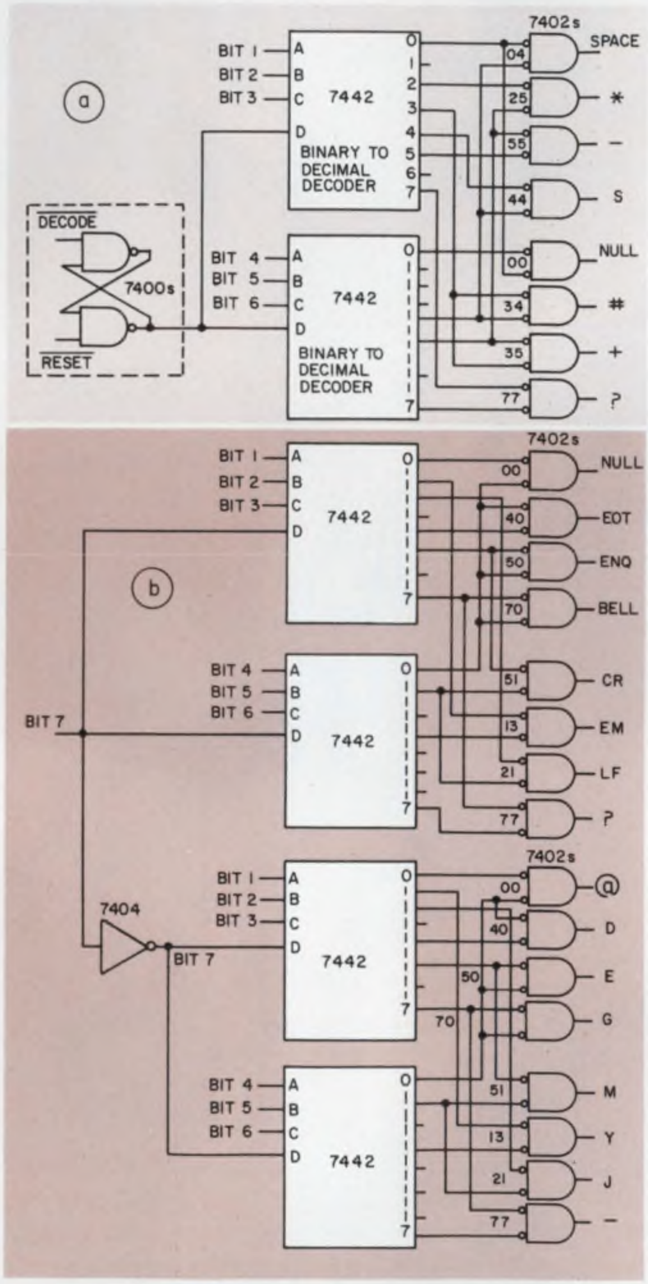
For recognizing up to three characters, single-character decoders are your best choice (Fig. 1). Not only are the components economical—$2.40 for three characters (Table 1)—they are also reliable.

The configuration in Fig. 1 is an example of a single-

**Robert J. Stetson,** Engineer, Storage Technology Corp., 9 Hampton Rd., Aurora, IL 60538.




1. **An eight-input NAND gate can detect specific ASCII 8-bit codes.** The NAND's output goes LOW only when the particular character or function code that the NAND is wired to recognize appears on the inputs.



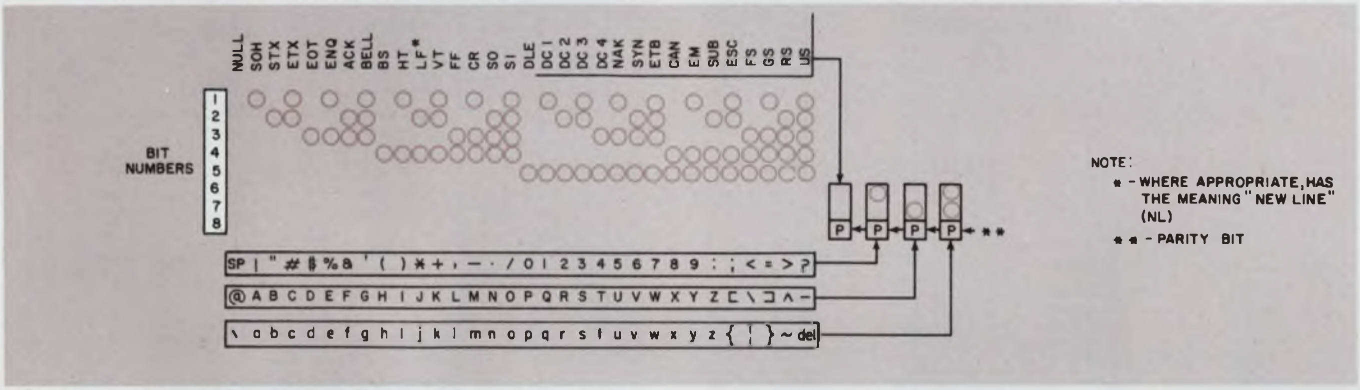

2. **To detect up to eight specific codes,** you can use two 7442 BCD-to-decimal converters (a). The detector operates on a modified ASCII 6-bit code, and provides a decode/reset function. But the circuit can recognize characters only from the number and function character sets. However, by foregoing the decode/reset function and using the seventh bit as part of the input code (b), the circuit can select from all four ASCII character sets.

# Table 1. Cost comparison of decoding circuits

| Decoding circuit | Recommended number of characters | Cost of circuit | Cost per character at max use | Special features |
|---|---|---|---|---|
| Fig. 1 | 1 to 3 | $ 2.40 | $0.80 | Simplicity hardwired |
| Fig. 2a<br>Fig. 2b | 4 to 8<br>16 | 3.04<br>5.76 | 0.38<br>0.36 | Small/low-cost hardwired |
| Fig. 3 | 8 | 11.04<br>15.04<br>18.96 | 1.38<br>1.88<br>2.37 | economy<br>medium-speed<br>high-speed<br>programmable |
| Fig. 4 | 9 to 20 | 13.00<br>17.00<br>20.10 | 0.65<br>0.85<br>1.05 | economy<br>medium-speed<br>high-speed<br>programmable |
| Fig. 5 | 21 to 30 | 15.90<br>19.80<br>24.00 | 0.53<br>0.66<br>0.80 | economy<br>medium-speed<br>high-speed<br>programmable |
| Fig. 6 | 128 | 74.28<br>94.72<br>113.92 | 0.58<br>0.74<br>0.89 | economy<br>medium-speed<br>high-speed<br>programmable |

Note: Price for 7400, 7402, 7404, 7408 and 7430 is taken as $0.36 each, and the 7442 at $1. EPROM 3702T prices used are $11, $15 and $19 each, respectively, for the economy, medium and high-speed versions.

# Table 2. The ASCII 8-bit code



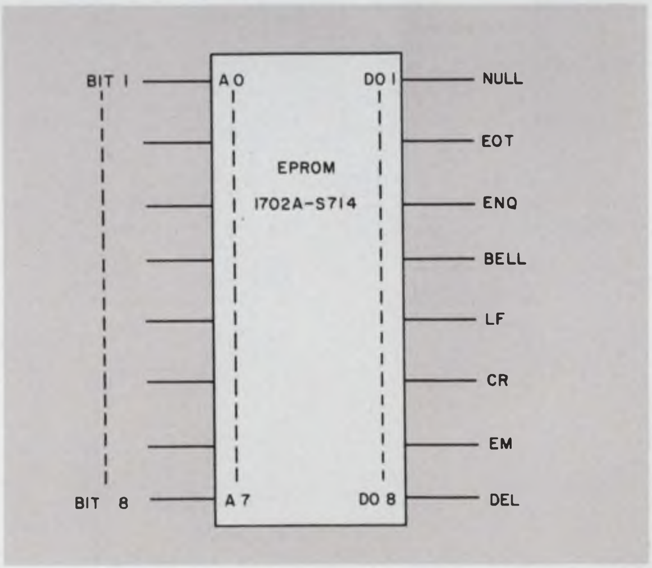

character decoder. It detects an even-parity ASCII Space code (Table 2). When bits 1, 2, 3, 4, 5, and 7 are LOW and bits 6 and 8 are HIGH, the output of the 7430 NAND gate goes LOW.

Above three characters, however, the number of chips, the PC-board area and interconnection effort needed for single-character decoders all become much too large. So, for decoding from four to eight characters, use a multicharacter decoder.

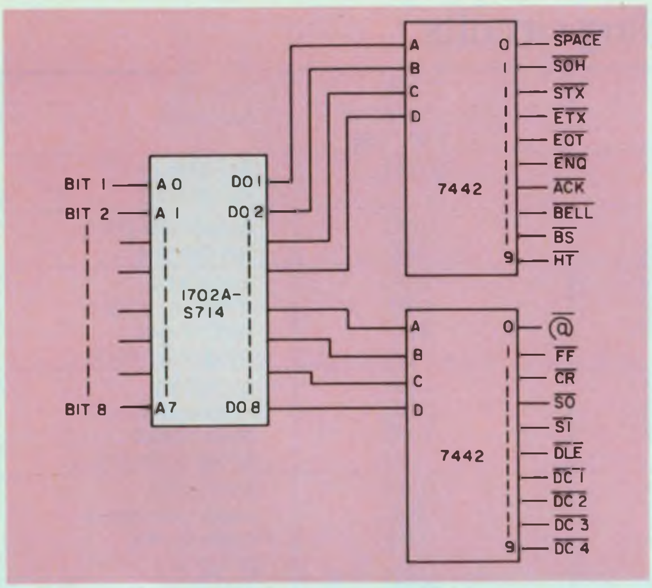
The simplest works with a 6-bit ASCII code (Fig. 2a). Input bits 1, 2 and 3 go to one 7442 BCD-to-decimal converter, and bits 4, 5 and 6 to another. The converter outputs represent two-digit octal numbers—00 to 77. When combined by a separate two-input 7402 AND gate for each character, these octal outputs provide HIGH outputs for selected 6-bit ASCII codes.

In 6-bit ASCII, since bits 7 and 8 of the standard 8-bit ASCII are left out, there is no parity feature (bit 8). Also, selections from only two of the four available function/character sets—for example, numbers and nontyping functions—can be identified (Table 2).

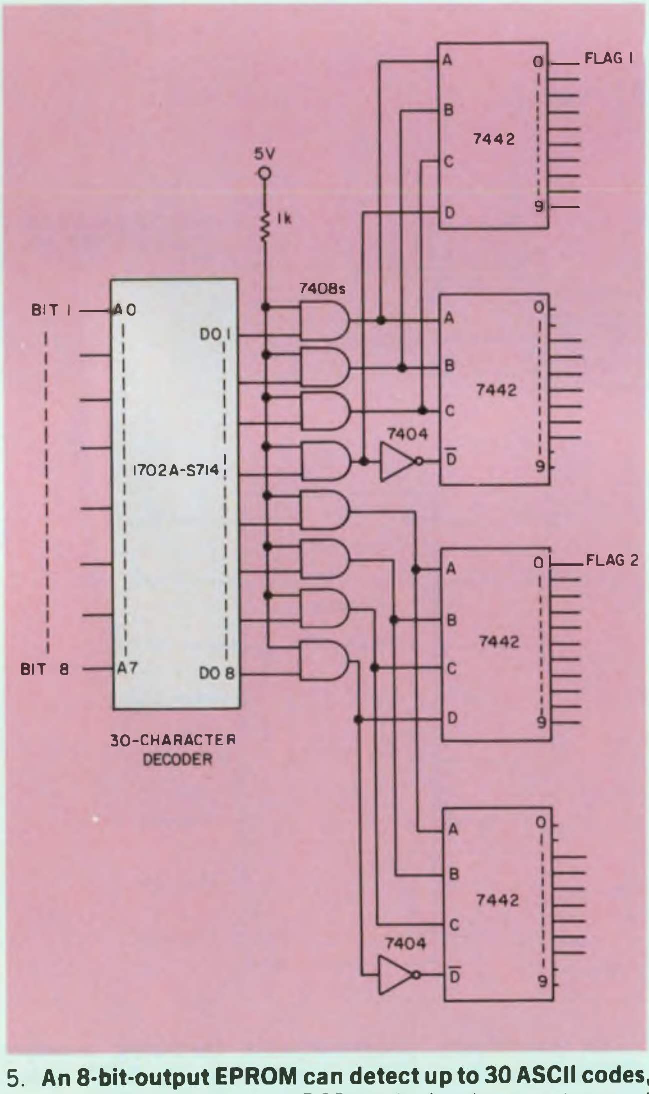
The Decode input to the control latch of Fig. 2a must



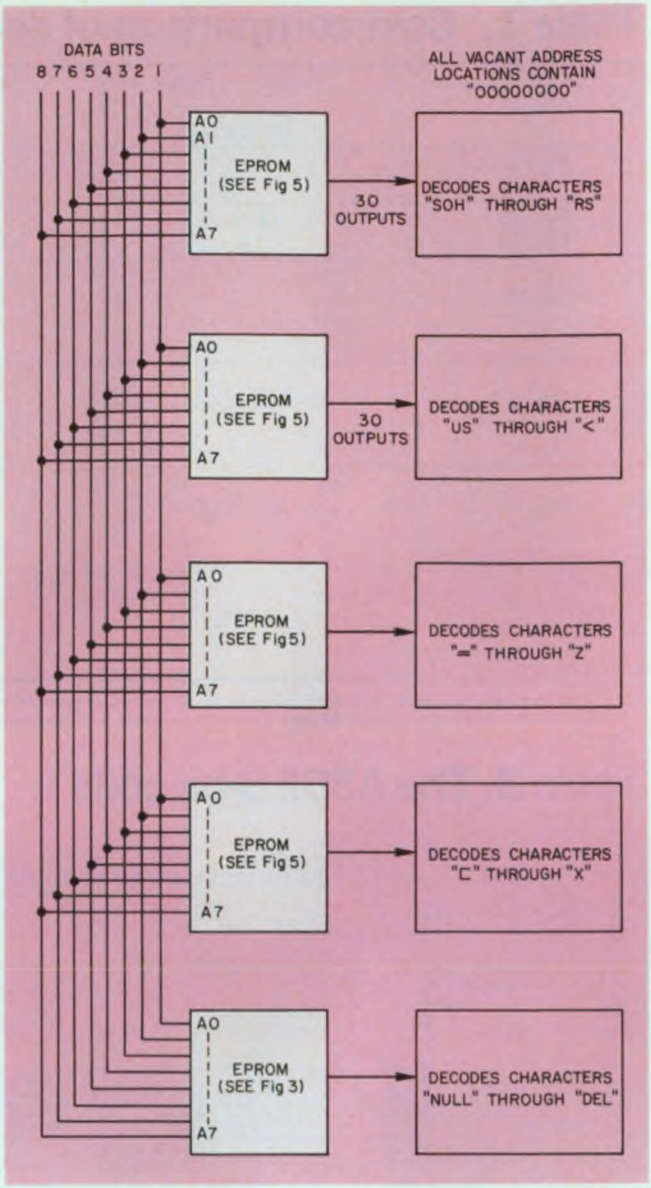

3. **An electrically programmable read-only memory (EPROM) can be used to recognize specific ASCII codes.** Proper programming even allows parity errors to be detected by appropriate use of bit-8's input to the EPROM.




4. **The decoding capability of an EPROM can be expanded with two BCD-to-decimal converters.** Up to 20 codes can be detected by separating the eight bits of an EPROM's output into two 4-bit hexadecimal numbers.




5. **An 8-bit-output EPROM can detect up to 30 ASCII codes,** when combined with four BCD-to-decimal converters and two inverters. Two extra outputs can be used as flags.




6. **All 128 ASCII codes can be recognized** with a configuration of four EPROM circuits, each arranged as in Fig. 5, and one EPROM circuit, as in Fig. 3.

be pulsed LOW to enable the decoder. With a circuit such as a universal asynchronous receiver transmitter, the latch is needed because the last character received must remain on the output of the UART and be decoded until the UART is reset. Where the duration of the output signal is not a factor, the latch may be eliminated and the 7442's D input grounded.

Or, as in Fig. 2b, the D input can receive bit 7, and operate with a 7-bit ASCII code. In this way, selections from all the ASCII characters or functions can be detected. However, bit 8, the parity bit, is still ignored.

### Firmware flexibility a bargain?

To accept a full ASCII 8-bit input, use a firmware decoder. An eight-character firmware decoder (Fig. 3) consists of an electrically programmable read-only memory (EPROM) that can accept eight input bits and provide a HIGH output for a desired code.

With the EPROM shown, you can program just eight decoded outputs. When programmed to detect a Null code—all input bits are LOW—only output $DO_1$ goes HIGH; outputs $DO_2$ through $DO_8$ remain LOW. Similarly, outputs that detect the other illustrated ASCII functions—EOT through DEL—go HIGH as their respective codes are applied to the EPROM's input, and the other outputs remain LOW.

Though the firmware circuit is more expensive than the circuits of Fig. 2, the flexibility of this decode arrangement can make it a better bargain. You can easily plug-in differently programmed chips and detect different codes, as well as program the $DO_8$ output to detect parity errors. Of course, with parity detection you sacrifice one of the eight EPROM outputs. As a result, the other functions may now have odd (or even) parity, and the parity-defective codes may be programmed to appear at, say, output $DO_8$.

The Intel 1702A and similar EPROMs can be erased by exposing them to 2523-Å ultraviolet light, and then electrically reprogrammed. A quartz lid on such units permits exposure to the ultraviolet.

The hardware of Fig. 2 can be used to expand the firmware of Fig. 3 to detect 20 codes (Fig. 4). If all 7442 inputs are HIGH, the 7442s don't activate any of their outputs. Consequently, you should program the EPROM so that all unused input codes produce a 11111111 output.

For 21 to 30 characters, however, you need two additional 7442s with an inverted bit to their D lines (Fig. 5). The EPROM's 8-bit output will then be able to represent two 4-bit hexadecimal numbers and recognize 30 characters with two codes reserved as "flags."

The flag signals can serve, for example, to disable character outputs to a printer, when nonprinting control functions are detected. Or they can limit output duration from a decoder by resetting a UART's output (as in Fig. 2). Note the 7408 gates that serve as EPROM-output drivers: The 1702A EPROM can drive only a single TTL load.

To go all the way and decode all 128 ASCII-8 codes, use the method in Fig. 6. Except for their programming, the EPROM circuits are identical to those in Figs. 3 and 5.

### Don't exceed your needs

EPROM prices vary, and it pays to shop around—Mostek, for example, has a direct replacement for the Intel 1702A units illustrated. EPROM access time is a major selection consideration and affects cost substantially. Don't buy more than you need. Note the effects of using economy, medium and high-speed versions within the same type number (Table 1).

Still, you may elect to use the decoders in Fig. 2 for more than eight characters. Or, you may decide to use Fig. 1, repetitiously, beyond three characters. Bear in mind that special requirements may override *all* the factors considered here and dictate the circuit you use. ■■

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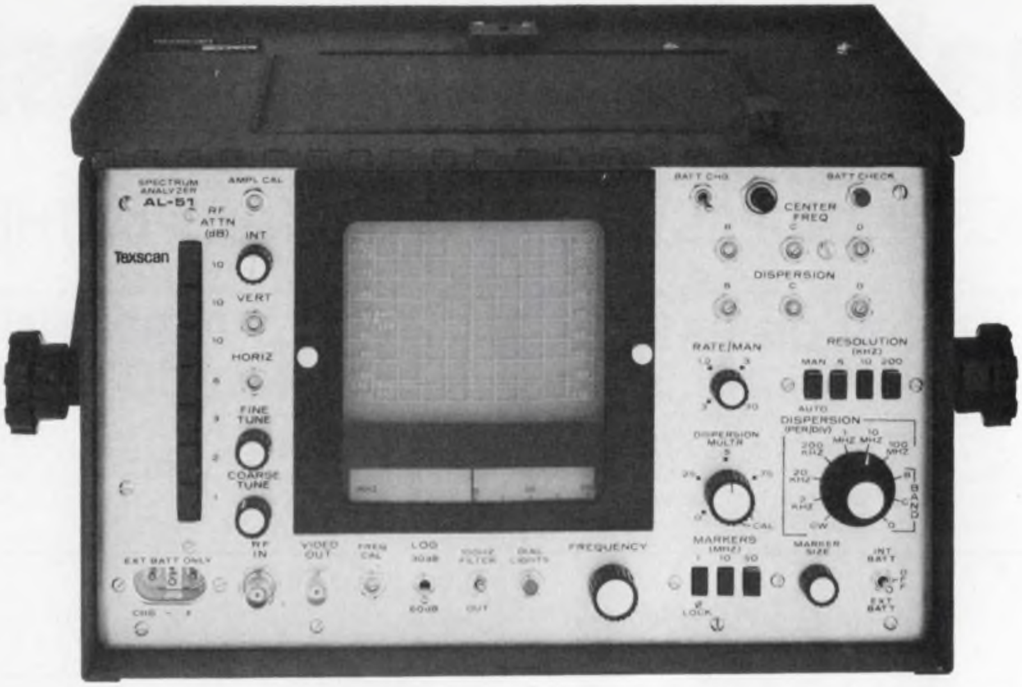
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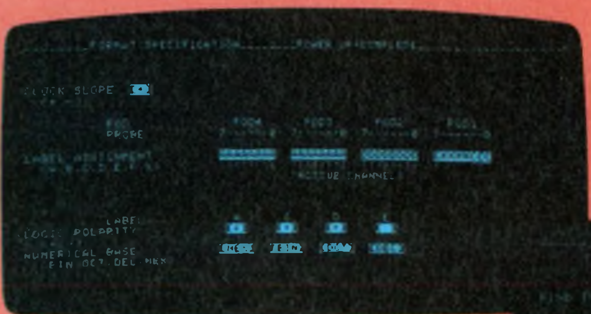
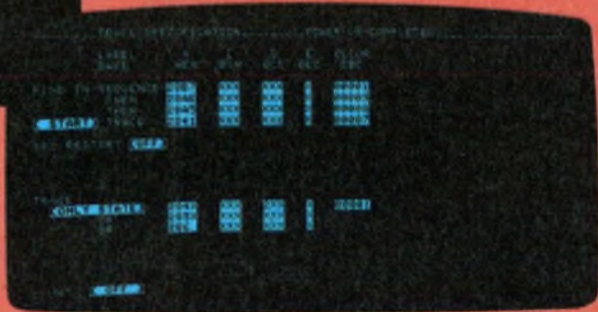


**Setup ease.** Inverse-video fields and moveable cursor in Format Specification mode direct you in defining clock slope, positive or negative logic and display formats (Hex, Binary, Octal or Decimal). You can also assign alphabetic labels to groups of data bits acting as a unit, greatly simplifying setups and display formatting. In addition, the display verifies probe-lead continuity and signals node activity.



**Complex measurement capability.** Fields and moveable cursor in Trace Specification mode simplify selection of trigger conditions and trace qualifiers. The ability to define up to seven sequential 32-bit words makes it possible to trace a specific path in complex branched programs. For further conditioning you can define the number of times each sequential state is to occur to allow the analyzing of looped or nested loop programs. And you can define up to seven states or groups of states for selective trace, simplifying data analysis and reducing the need for deep memory.

**Simplified interpretation.** List Display shows you trigger words plus the program flow you specified in the set-up specifications. Now you can easily compare operating software to original source listings or, in the trace-compare mode, to program flow stored in the 1610A memory.

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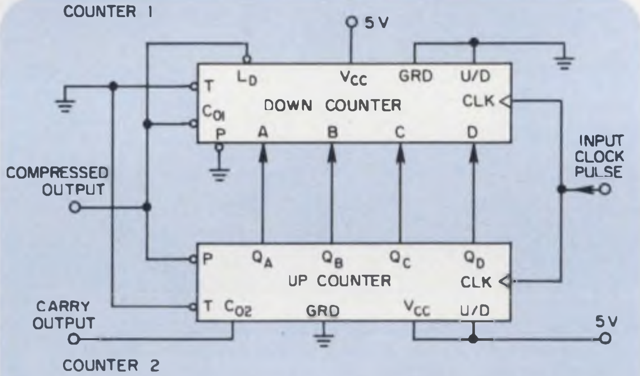
# Obtain a compressed counting range with a variable-modulus counter

Quite frequently pulse-train inputs to programmable devices such as microprocessors exhibit wide dynamic ranges. Since, in most cases, resolution requirements at higher frequencies are not as stringent as at lower rates, a nonlinear frequency transfer function can relieve the burden on the system intelligence. A variable-modulus counter to compress the counting range can perform such a task (Fig. 1).

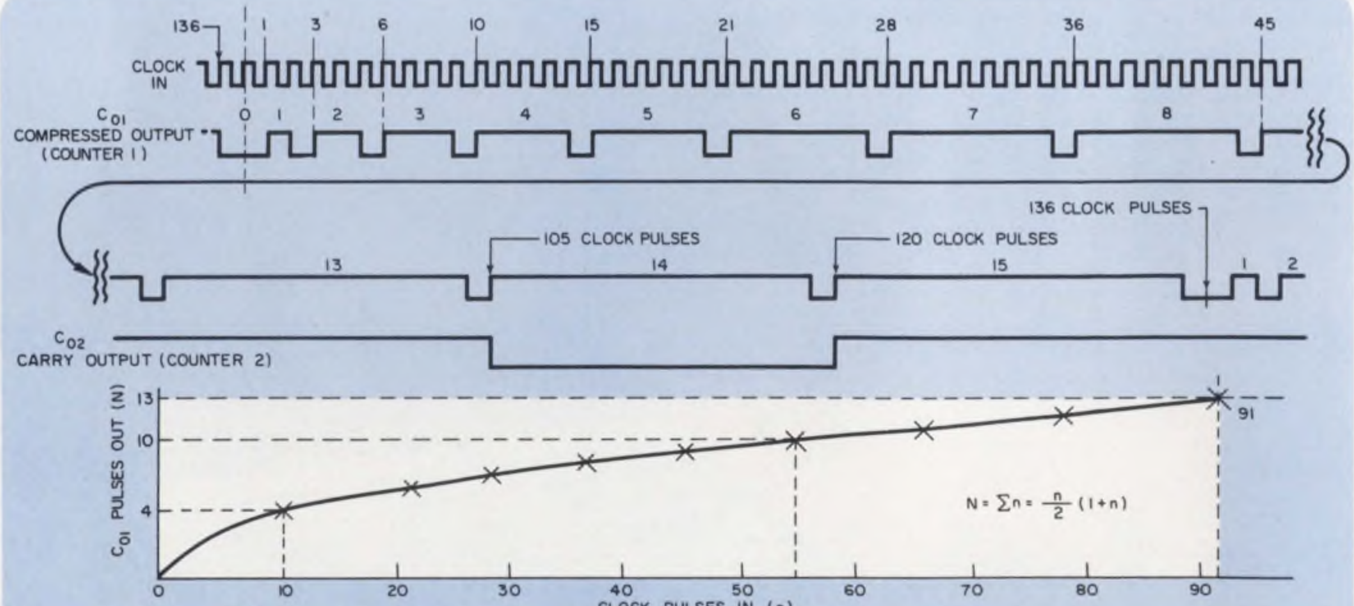
The circuit consists of two presettable up/down counters. Counter 1 counts in the down mode, while Counter 2 counts up. When the output of the latter presets the former, a varying-modulo counter is achieved: The modulus of the down counter becomes equal to the number previously loaded into it from the up counter.

The range can be expanded either by cascading the circuit or by increasing the lengths of the counters. And various complex transfer functions can be achieved by inserting appropriate logic or a PROM between the outputs of Counter 2 and the inputs of Counter 1.

*Charles B. Mitchell, Senior Engineer, National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051.* CIRCLE NO. 311




**1. Nonlinear counting is achieved** when the up counter loads the down counter and thereby determines the down-counter's modulus.




**2. A compressed output of the number of input clock pulses** is obtained at the down counter's carry output, $C_{01}$. This output is the sum, N, of the arithmetic progression of the input clock pulses, n.



CIRCLE NUMBER 48 ▶

# 555-timer circuit generates ultra-low-frequency signals

Using only small capacitors, the three 555 timers in the circuit of Fig. 1 can generate ultra-low frequencies—as low as $10^{-3}$ Hz.

Timers $T_1$ and $T_2$ operate in monostable modes, and $T_3$ operates in a free-running astable mode. During the interval when $T_3$'s pin-3 output is LOW, transistor $Q_1$ conducts and capacitor $C_3$ charges through $R_3$ (Fig. 2). When the $T_3$ output goes HIGH, $Q_1$ cuts off and $C_3$ maintains the previously accumulated charge. This process repeats as $T_3$ oscillates until $C_3$ charges to $(2/3)V_{cc}$, which forces $T_1$'s pin-3 output LOW and triggers $T_2$'s pin 3 HIGH via $C_2$.

Now, the roles of $T_1$ and $T_2$ are interchanged and the process is repeated, with $C_4$ charging through $Q_2$ and $R_4$.

The time required for $C_3$ and $C_4$ to charge to $(2/3)V_{cc}$ is determined by the following equations:

$$T_1 = 1.1R_3C_3\ [2+(R_5/R_6)],$$

and

$$T_2 = 1.1R_4C_4\ [2+(R_5/R_6)].$$

Therefore, the frequency is

$$F=(T_1+T_2)^{-1}.$$

And when $R_3C_3=R_4C_4$, then

$$f=\frac{1}{2.2R_3C_3\ [2+(R_5/R_6)]}.$$

The over-all frequency is adjusted by $R_5$, and the "half" periods by $R_3$ and $R_4$. With

$$R_3=R_4=500\ k\Omega,$$
$$C_3=C_4=2\ \mu F$$

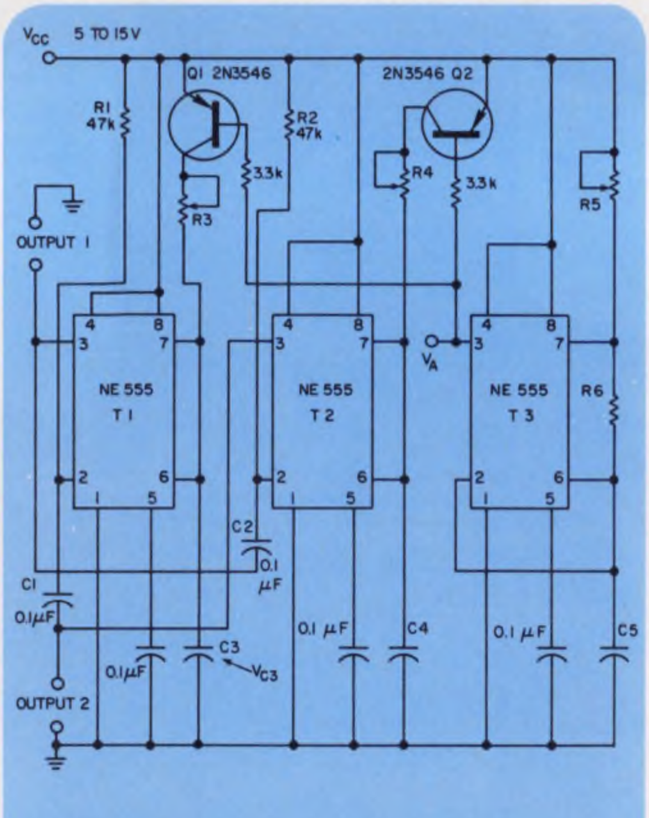
and

$$R_5/R_6=48,$$

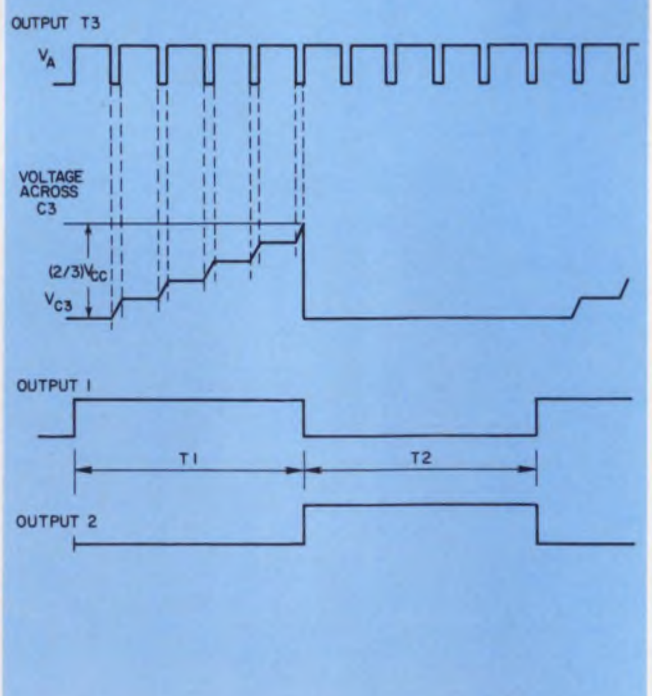
then

$$F=9\cdot 10^{-3}\ Hz.$$

*Cedomir Milosavljevic, Elektronska Industrija, Research & Development Institute, 18000 NLS, Yugoslavia.* CIRCLE NO. 312




1. **Ultra-low frequencies can be generated** with this circuit, and only small capacitors are needed.




2. **Timer $T_3$ runs freely and builds voltage across $C_3$** in steps until $(2/3)V_{CC}$ is reached. Then $T_1$ turns on and $C_4$ is charged in steps. The cycle continuously repeats between $T_1$ and $T_2$.

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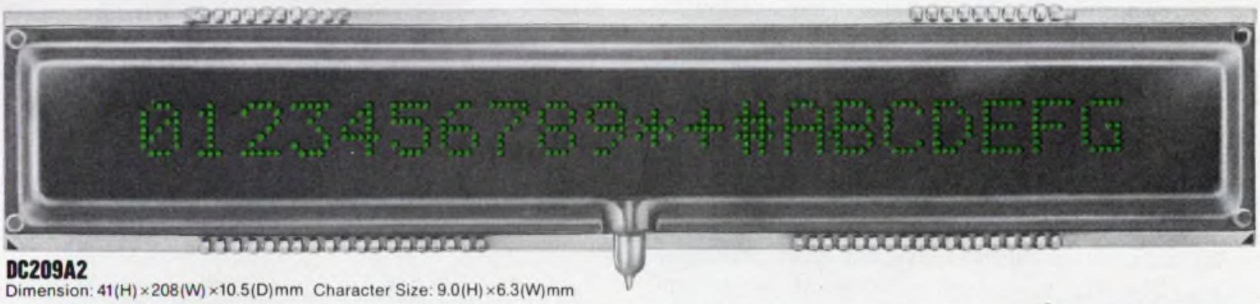
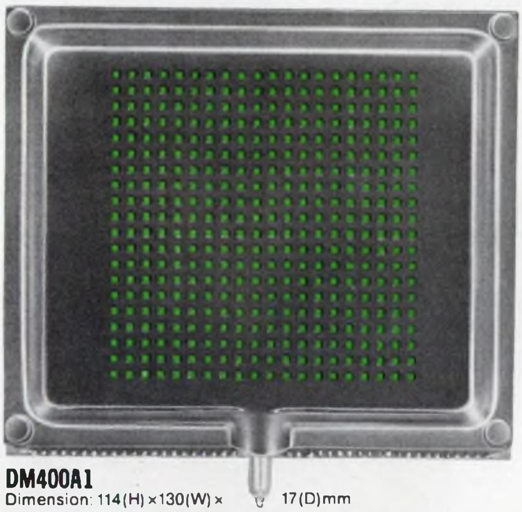



**DC209A2**
Dimension: 41(H)×208(W)×10.5(D)mm Character Size: 9.0(H)×6.3(W)mm

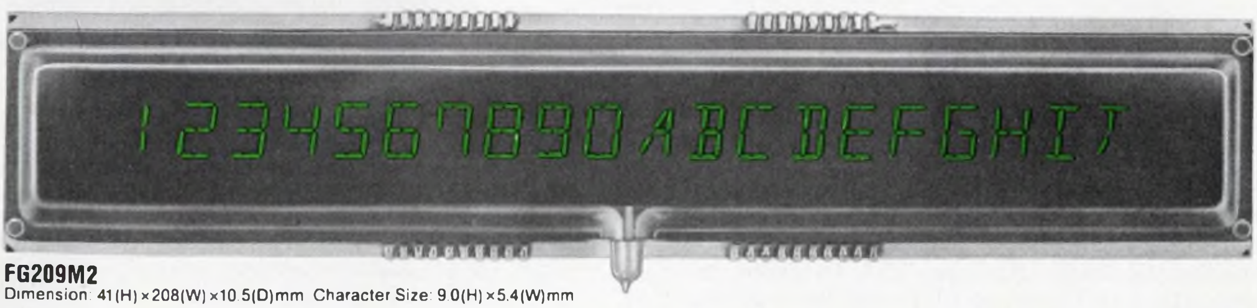


**DM400A1**
Dimension: 114(H)×130(W)× 17(D)mm


**DC95A2**
Dimension:
24(H)×75(W)×7.2(D)mm
Character Size:
5.05(H)×3.55(W)mm


**FG48D6**
Dimension:
25.5(H)×56.5(W)×7(D)mm
Character Size:
8.0(H)×4.2(W)mm

**FG120S1**
Dimension: 39(H)×138(W)×12.5(D)mm




**FG209M2**
Dimension: 41(H)×208(W)×10.5(D)mm Character Size: 9.0(H)×5.4(W)mm

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**Taipei**
72-9 SEC 2 JEN AI RD., Taipei
Phone: 351-0293 Telex: 11176

*Manufacturer:*
**ISE ELECTRONICS CORP.**
P.O. Box 46 Ise-shi,
Mie-Pref., Japan
Phone: (05963) 5-2121 to 4
Telex: 4969523

CIRCLE NUMBER 50

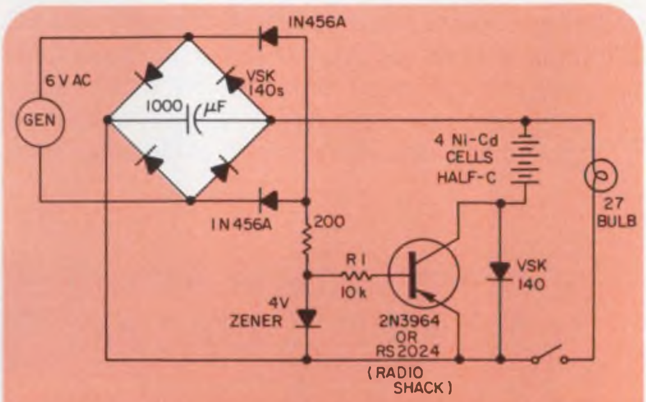
# Schottky diodes rectify efficiently in a bicycle-lighting system

For bicycle-lighting systems, four half-C-sized nickel-cadmium cells can fit neatly in the space designed for two ordinary C-sized carbon-zinc batteries and provide a 5-V, 0.75-Ah source. Change the No. 14 lamp normally used with the two C-cells to a No. 27 (4.9 V at 0.3 A) or No. 425 (5 V at 0.5 A) lamp and you can convert a candle glow to a blazing torch that permits the bicycle night-rider to travel with greatly increased safety.

Charging the nickel-cadmium cells with a 6-V-dc power supply is straightforward. However, make sure to limit the charging current to less than 70 mA with a suitable series resistor. Though this arrangement is satisfactory, charging the cells automatically while riding is far more convenient.

For an automatic lighting system that produces little drag, the Sturmey-Archer Dynohub generator is recommended over friction driven types. But for either type the circuit in the figure can be used to rectify and regulate the battery-charging current. Friction-driven generators, although they can deliver more power and are cheaper, cause substantial drag and produce wear on the tires.

Conversion efficiency of the circuit is high because Schottky diodes (VSK-140) reduce the bridge-rectifier voltage drops from about 1.2 V developed across ordinary silicon diodes to less than 0.6 V. Charging current with the light switched off is limited to 60 mA by the transistor. A VSK-140 diode bypasses the current-limiting transistor when the bicycle generator can't provide full lamp current. The action of this diode allows the circuit to switch smoothly from battery power to generator power, and vice versa.




**A battery-charging circuit for a bicycle lighting system** uses Schottky diodes for high efficiency.

The only critical component value is $R_1$. It is chosen to limit charging current with the lamp switched off to less than 70 mA, when the bicycle is moving at top speed. Although $R_1$'s initial value can be determined by merely spinning the generator's drive wheel, road testing should be used to verify proper operation.

*Chesley H. Looney Jr., Equipment Management Officer, NASA, Goddard Space Flight Center, Greenbelt, MD 20771.*

CIRCLE NO. 313

---

**IFD Winner of March 1, 1977**
**Harry L. Latterman,** Digital Design Engineer, Courier Terminal Systems, 2202 E. University Dr., Phoenix, AZ 85038. His idea "TTL Oscillator Interfaces Data for Display by a Television Set" has been voted the Most Valuable of Issue Award.

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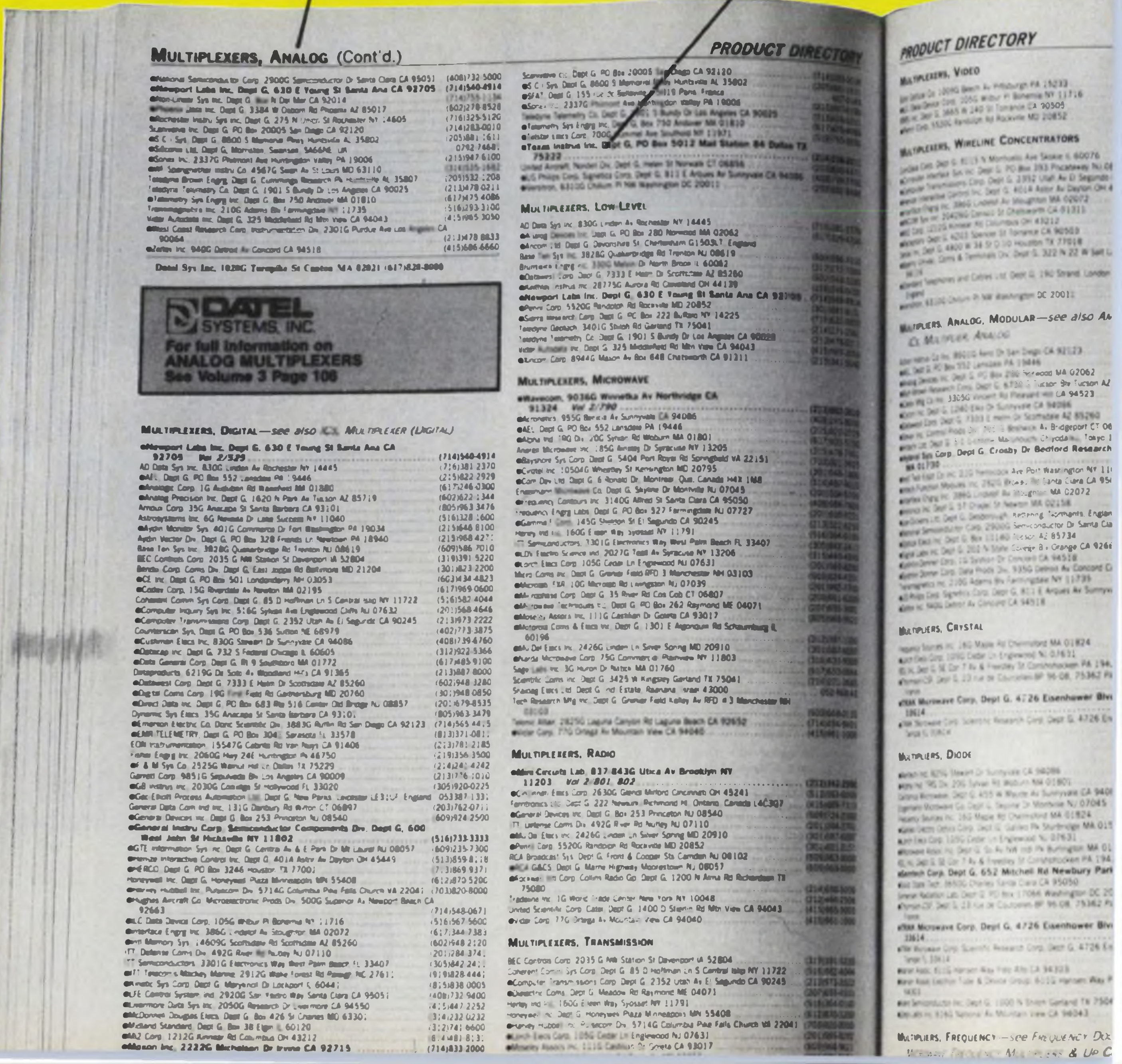
Boldface type and page references steer you immediately to catalog data the manufacturer has supplied for you in Section 2 of the GOLD BOOK.



# makes your life easier

## ECTRONICS **PRODUCT DIRECTORY** IN THE WORLD!

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This symbol, "•", separates the serious from the would-be manufacturer. It means the company has submitted literature to us describing the product.

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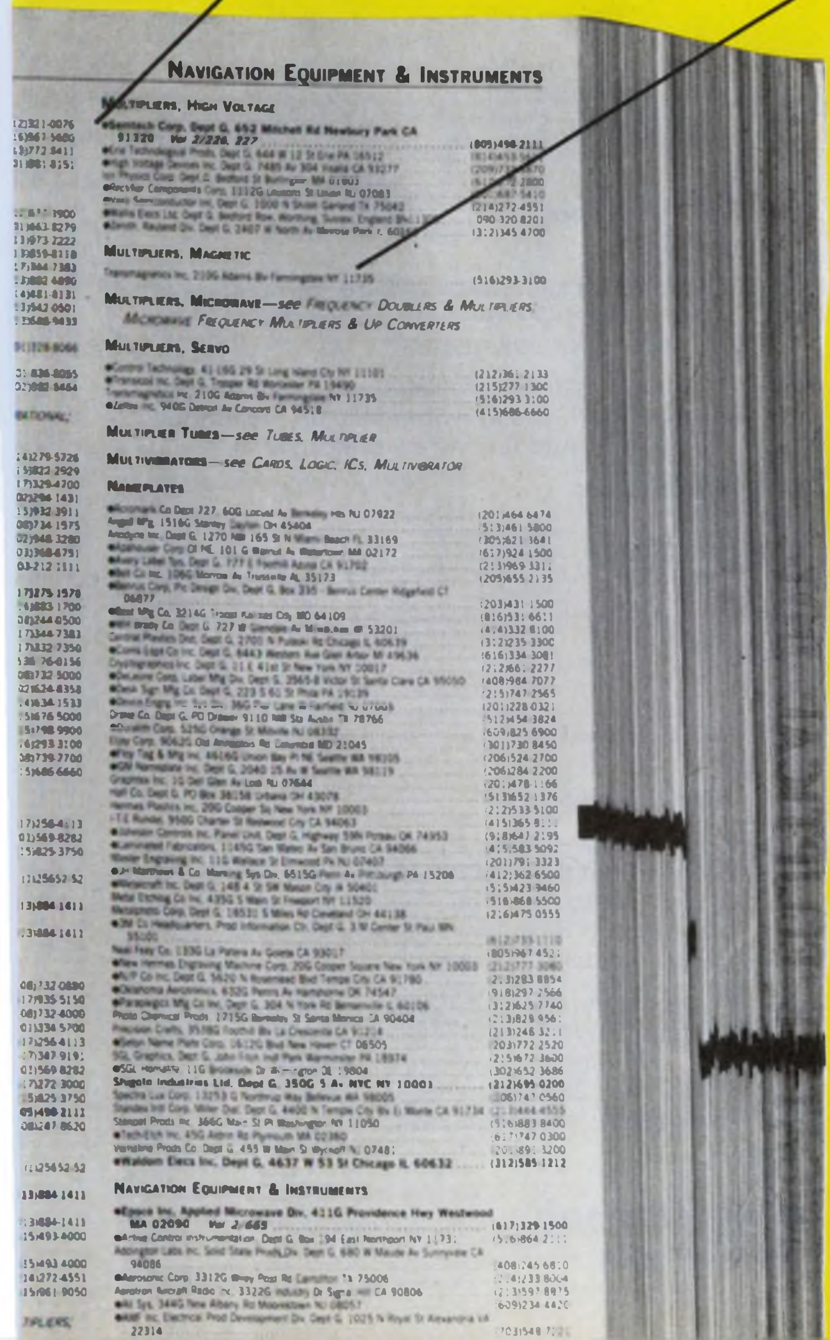


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### WANT TO FIND OUT WHO MAKES WHAT?

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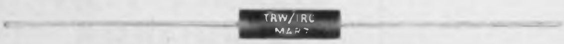
# TRW's MAR™ ultra stable resistors. Performance plus.

Our ultra-precision MAR resistors match the performance of precision wirewound, *plus* they give the inherent advantages of TRW metal film.

Like smaller size, better frequency response, higher resistance values and lower cost.

And MAR's are not "selected" from a lower grade process. The entire facility was *designed* to yield *only* high accuracy devices.

And it *DOES:*




### MAR axial lead family

Tolerances to ±.01%. TC's ±5 to 25 ppm/°C. Where speed and precision count, the MAR does it all. In a dimensionally clean, axial lead molded package.

With the non-measurable noise, low voltage coefficient, load stability, resistance/size ratio and *reliability* of our metal film process.

*Plus* MAR matched sets and packaged networks have tolerance and TC matching to ±.005% and 1 ppm/°C.

**Specifications**

| IRC Type | Resistance Range* (Ohms) | Temperature Coefficients −20°C to +85°C (±ppm/°C) | Tolerances (±%) | Power Rating** @ 85°C (Watts) | Voltage Ratings (Volts) |
|---|---|---|---|---|---|
| MAR3 | 20 – 100K | T10 = 15 | 1.00, 0.50, 0.25, | 1/20 | 200 |
| MAR5 | 20 – 250K | T13 = 10 | 0.10, 0.05, 0.02, | 1/10 | 250 |
| MAR6 | 20 – 500K | T16 = 5 | 0.01 | 1/8 | 300 |
| MAR7 | 20 – 1 Meg | | | 1/4 | 500 |

*Wider ranges available, contact factory.
**Higher power ratings available. Contact factory.


### AR40 radial lead devices

This plug in configuration offers absolute accuracy and documented reliability. TC's to ±2ppm/°C, tolerances to ±.01% are standard.

*Plus,* AR40 uses only .03 in.² PCB area including lead attachment, and has the same mechanically rugged terminations used on all MAR resistors.

**Specifications**

| TCR Class. | Standard Temp. Coeff. (°C) | Resistance Range* (Ohms) | Standard Tolerance (±%) | Wattage 85°C |
|---|---|---|---|---|
| T-18 | 2 ppm 0 to 60°C<br>5 ppm −55 to 125°C | 20 to 100K | .01, .02, .05, .10, .25, .50, 1.00 | .3 watts |
| T-16 | 5ppm 0 to 60°C<br>10 ppm −55 to 125°C | | | |

*Wider ranges available, contact factory.

### AR90 high range resistors

Designed for applications where you need values up to 10 Meg Ohms—such as precision voltage dividers, input attenuators.

*Plus,* despite its high resistance range, the AR90 has standard TC's to ±5ppm/°C and tolerances to ±0.05%. And it is a *real* space saver.

**Specifications**

| IRC Type | Resistance Range* (ohms) | Temperature Coefficients −20°C to +85°C (±PPM/°C) | Tolerances | Power Rating | Voltage Rating |
|---|---|---|---|---|---|
| AR90 | 1M – 10M | T10 = 5<br>T13 = 10<br>T16 = 15 | 1.0, 0.5, 0.25, 0.1, 0.05 | .5W | 1000 |

*Wider ranges available. Contact factory.

### Need prototypes fast?

TRW has on stream another *big plus*—a short order production line (in addition to our regular facility) designed to give you quick delivery on bread board quantities. Delivery to satisfy your needs, typically 2-3 weeks.

For more information on ultra-precision resistors, contact TRW/IRC Burlington. TRW/IRC Resistors, an Electronic Components Division of TRW, Inc., 2850 Mt. Pleasant St., Burlington, Iowa 52601. (319) 754-8491.

**TRW IRC RESISTORS**

CIRCLE NUMBER 52

# Four very small ways to improve on your PC design.

With four types of switches—rockers, pushbuttons, toggles and DIPs—Cutler-Hammer offers one of the industry's broadest and most unique selections of PC subminiatures.

Each of the hundreds of available styles provides the reliability you've come to expect from Cutler-Hammer. With ratings to 6 amps, each conforms to standard circuit board mounting requirements.

PC switches, along with accessories and decorative hardware, are distributor stocked for local availability. And since most are manufactured in the United States, we offer fast reaction time on solder lug and wire wrap terminal variations, as well.

To improve your next design in any number of small ways, contact your Cutler-Hammer Sales Office or Switch Distributor.

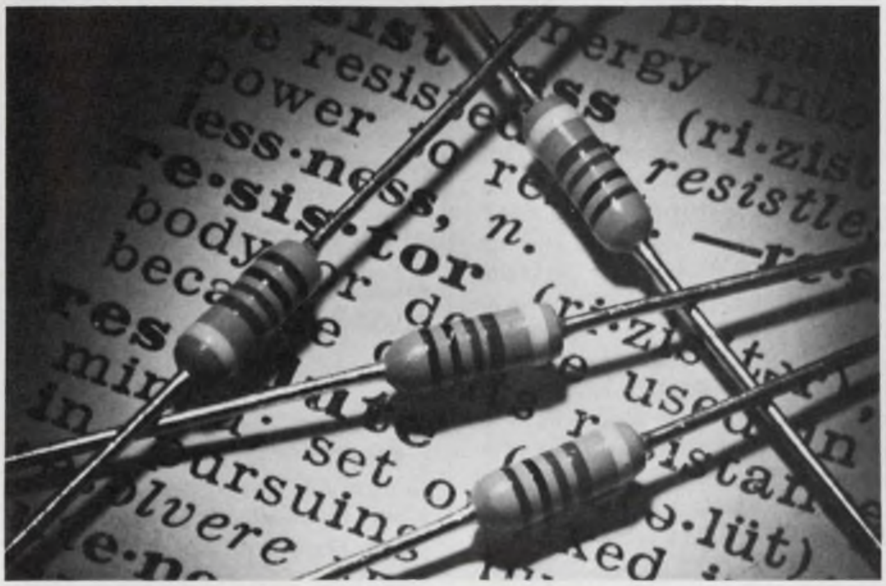

Switch to No.1

**CUTLER-HAMMER**

*SPECIALTY PRODUCTS DIVISION, Milwaukee, Wis. 53201*

**CIRCLE NUMBER 54**

# Metal-film 2% 1/4-W-sized resistors cover 10 Ω to 22 MΩ and handle 350 V to 1/2 W



*MEPCO/Electra, Inc., Columbia Rd., Morristown, NJ 07960. John E. Covey (201) 539-2000. P&A: See text.*

MEPCO's GPR 5000X general-purpose resistors are the only metal-film units with a 350-V maximum working voltage and 2% tolerance that cover the total 10 Ω to 22.1-MΩ range in one 1/4-W body size.

Allen-Bradley's cermet Type CC, 2% resistors are almost identically rated —same size and resistance range—and they have a lower TC (±100 ppm/°C vs ±200 ppm/°C for the GPR 5000X). But the working voltage is a lower 250 V. A spokesman for Allen-Bradley admitted that the company prefers to concentrate on its 1%, ±50 to ±100 ppm/°C units, although the 2% units are readily available on order. He wouldn't give a price, but said that it is "competitive."

Other resistor manufacturers, such as Corning, TRW/IRC and Dale, offer competitive metal-film resistors, but they don't cover the total resistance range, and they come in larger body sizes for the higher ranges.

Although the MEPCO resistors' body size, 0.3 (L) × 0.098 (D) in., max corresponds approximately to the MIL-R-22684, RL07 1/4-W-sized resistors, the 5000X resistors can handle 1/2 W at 70 C and 1/4 W at 125 C. Therefore in some applications, this one size can cover both the RL07 and RL20 (1/2 W) sizes.

To give the user an idea of the performance he can expect of the resistors, MEPCO has supplied a comparison with MIL-R-22684 requirements (see table). But careful: the term "typical" in the table isn't defined.

In addition to these apparently excellent stability properties, metal-film resistors generally provide better overall operating specs than the closest performance rival—carbon-film resistors: low noise, about 0.5 μV/V vs 10 μV/V at 1 MΩ; low voltage coefficient, 0.05 ppm/V vs roughly −5 ppm/V; and tighter TCs, ±50 to ±200 ppm/°C max vs −200 to −500 ppm/°C.

Available from stock, in million quantities the GPR 5000X resistors cost $27 vs approximately $32 per thousand for equivalent 2% resistors—over narrower resistance ranges—from Corning, TRW or Dale, according to MEPCO. Carbon-film resistors, to about 1 MΩ with about a −500 ppm/°C TC, are priced at about $20 per thousand.

MEPCO also offers 1% versions of the metal-film units (SPR 5000X), which are somewhat lower in cost than Allen-Bradley's 1% Type CCs. MEPCO's resistors sell for about $36 per thousand; Allen-Bradley's go for about $42 per thousand.

| | |
|---|---|
| MEPCO | CIRCLE NO. 302 |
| Allen-Bradley | CIRCLE NO. 303 |
| Corning | CIRCLE NO. 304 |
| Dale | CIRCLE NO. 305 |
| TRW/IRC | CIRCLE NO. 306 |

| Tests per MIL-R-22684 | Max. % change in resistance | |
|---|---|---|
| | MIL-R-22684 requirements | GPR5053X typical |
| Temperature cycling, −65 to +150 C | 1.0% | 0.10% |
| Low temp oper, −65 C | 0.5 | 0.02 |
| Short time overload | 0.5 | 0.02 |
| Terminal strength, 5 lb load | 0.5 | 0.02 |
| Dielectric withstanding volts | 0.5 | 0.01 |
| Resistance to solder, 350 C | 0.5 | 0.01 |
| Moisture resistance* | 1.5 | 0.25 |
| Life (1000 h) | 2.0 | 0.25 |
| Shock, med impact, 50 G, 11 ms | 0.5 | 0.01 |
| Vibration, high freq 10-2000 Hz | 0.5 | 0.01 |

*Per MIL-R-10509

## Ceramic chip capacitors rated to 4000 WVDC

*Johanson/Monolithic Dielectrics Div., Box 6456, Burbank, CA 91505. (213) 848-4465. $0.40 to $3.85 (1000 qty.); stock to 6 wks.*

High-voltage ceramic chip capacitors operate to 4000 WVDC. Available in NPO/COG or BX/X7R dielectrics, the units come in five sizes from 0.15 × 0.15 × 0.12 in. to 0.54 × 0.40 × 0.12 in. with capacitance values up to 0.82 μF. Standard models are rated 1000, 2000, 3000 and 4000 WVDC.

CIRCLE NO. 307

*COMPONENTS*

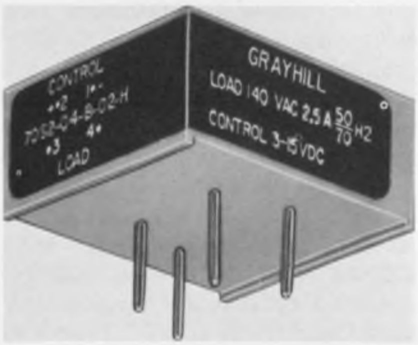
## Precision potentiometers linear to 1%

*Bourns, Inc., 1200 Columbia Ave., Riverside, CA 92507. (714) 781-5122. About $6 (OEM qty); stock.*

A pair of 1%-linearity potentiometers, single-turn Model 6537 servomount and Model 6637 bushing-mount, are built with few parts and simple construction. Other features include a one-piece precious-metal wiper, instead of a less-reliable two-piece type; silver deposited between the molded-in terminals and element to protect against shock; and low-temperature fired and thermally swaged connections in place of solder, conductive epoxy or silver cement.

CIRCLE NO. 308

## Tiny relay handles surge currents to 100 A




*Grayhill, 561 Hillgrove Ave., La Grange, IL 60525. Ed Langille (312) 354-1040. $12.60 (100 qty); stock.*

Taking up less than 0.6 in.$^3$, the Micro Cube solid-state relay offers a switching capability of 2.5 A at 25 C and withstands a 100-A surge for one cycle. A height of only 0.475 in. allows the relay to be mounted on racked PC boards. The optically isolated unit can take 400-V transient pulses and has a 3000 V/$\mu$s dV/dt rating. The unit is designed to work with inductive loads. The logic-compatible input circuit operates on 3 to 5 V dc with a 14-to-30-V-dc range available as an option. Termination is on 100-mil centers.

CIRCLE NO. 309

## Miniature pots have rotary switches

*Centralab, P.O. Box 858, Highway 20 West, Fort Dodge, IA 50501. (515) 955-8534. $0.75 (1000 qty); stock.*

The Series-900 miniature potentiometers now come with rotary switches. Designed for snap-in installation, the units are rated for 6.5 A at 1.5 V dc and 0.2 A at 45 V dc. The snap-action switches are spst normally open or normally closed at the cw or ccw end. Over-all mounted dimensions are 7/8 in. dia × 1/2 in. Hot stamped numbers on the colored thumbwheel edge are available as an option.

CIRCLE NO. 310

## At 20 kHz, transformer shrinks size and weight

*Stevens-Arnold, 7 Elkins St., South Boston, MA 02127. (617) 268-1170. From $12.75 (100 qty); 4 wks.*

IT-3573 20-kHz converter transformers are only 1/20th the size and 1/40th the weight of equivalent 200-W, 60-Hz transformers. They measure 1.81 × 1.56 × 1.375-in. seated height and weigh 4 oz. Two columns of PC header pins, spaced 0.9-in. apart, provide the connections. An efficiency of 98% permits up to 200 W of output power with a single secondary and 150 W with multiple secondaries. The transformer operates from a nominal 100 V (200 V max) at a 20-kHz square-wave input. Optional shielding is available.

CIRCLE NO. 320

## Mercury-film relay contacts don't bounce

*InResCo, 503 Adamston Rd., Brick Town, NJ 08723. (201) 477-5454. $3.25 (1000 qty); 4 to 6 wks.*

The HGM bounce-free, mercury-film relay is SPTD and handles rated loads of 2 A at 5 V dc, 1 A at 24 V dc or 0.1 A at 200 V dc. Maximum contact breakdown is 600 V dc; maximum switch cycle rate is 100 cycles; and the dc contact resistance is 0.15 Ω with a resistance stability of 0.02 Ω. The relay is shock resistant to 50 g's and vibration resistant to 20 g's (10 to 2000 cycles). Designed for PC-board mounting, the relay measures 3/4 × 5/8 × 3/4 in.

CIRCLE NO. 321


# Three ways to make your systems more cost-effective:

We make three different disc storage drives for OEM use. Each has been designed to make it the most cost-effective drive you can use. To help you build computer systems that perform better for your customers; return more profit to your company.

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Clip and mail to Memorex, Small Systems Div., San Tomas at Central Expwy., Santa Clara, CA 95052 or phone (408) 987-2928.

CIRCLE NUMBER 56

## Graphics terminal plots, stretches, zooms & pans

*Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, CA 94304. (415) 493-1501. P&A: See text.*

The first graphics terminal from HP, the 2648A, weighs in with a number of features usually associated with more expensive, dedicated machines:

■ Raster scanning for a bright, selectively erasable display.

■ Independent memories for alphanumerics and graphics, which permit a lot of leeway in picture and dialogue manipulation.

■ Automatic plotting of tabular data, which avoids extensive and costly software.

■ Picture zooming to as much as 16-times magnification and panning of any picture portion not displayed.

■ "Rubber-band" capability for drawing and stretching lines to any length in any direction.

All those features will set you back just $5500, yet the µP-controlled (8080)

2648A offers even more—like a data-communications interface (RS 232), user-defined keys and off-line editing, among other features.

The unit's 5 × 10-in. display presents data in a 24-line × 80-column format, with alphanumerics made up of 9 × 15-dot cells. Sixteen 16-k RAMs provide a graphics resolution of 360 × 720 dots. For still more graphics power, you can spend another $1600 and get two built-in tape drives with 220 kbytes of storage.

CIRCLE NO. 301

## Four-in-one analyzer offers 27 test modes

*Rockland Systems, 230 W. Nyack Rd., West Nyack, NY 10994. (914) 623-6666. Series III $8900; 45-60 days.*

Model FFT 512/S-Series III spectrum analyzer combines four capabilities in a single instrument: a real-time narrowband spectrum analysis covering the 0- to-100-kHz range; 1/3-octave and full-octave analysis, both implemented by banks of precise digital filters; and tunable rms voltage/power measurements displayable as V rms, (V rms)$^2$, and dB V (relative to 1 V or to a selected reference). The four capabilities provide some 27 modes of operation.

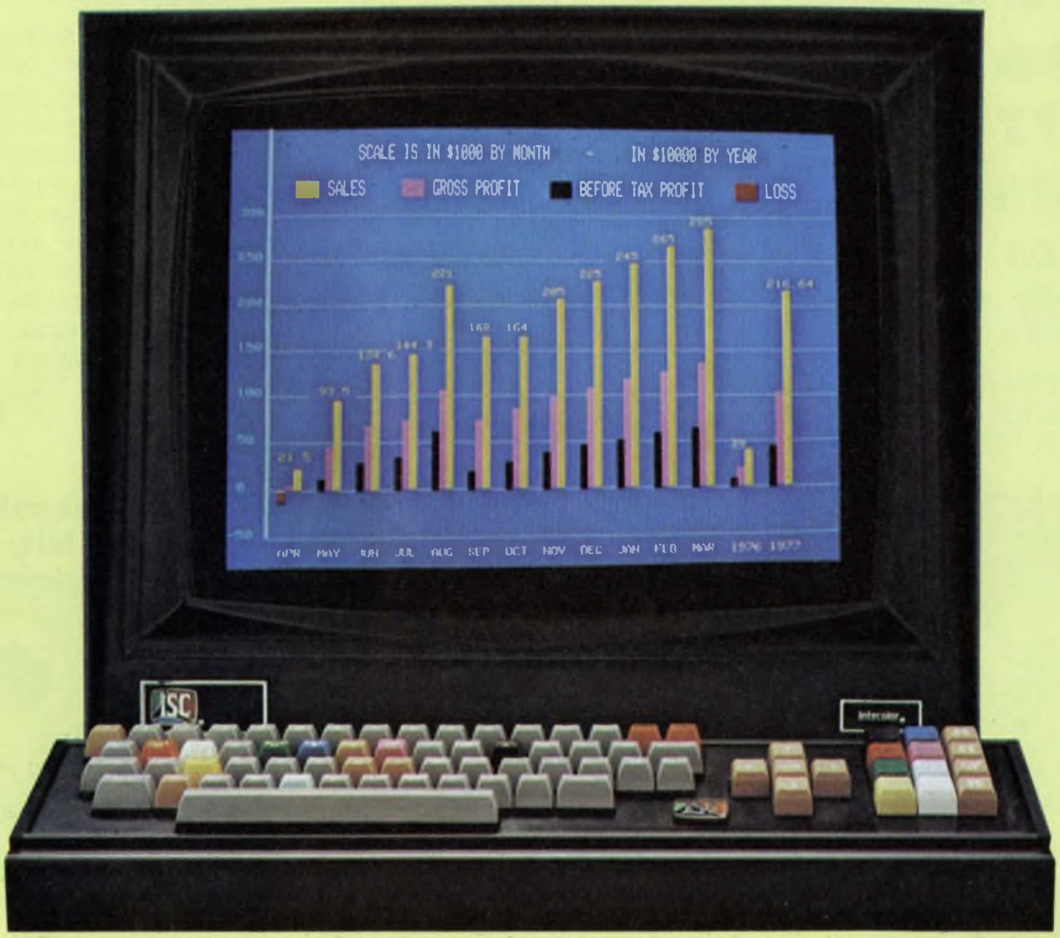
CIRCLE NO. 322

## Unit interfaces scope to plotter or recorder

*Gould-Advance, Raynham, Rd., Bishops Stortford, Hertz. CM23 5 PF, England.*

An automatic hard-copy output unit, the 4002, used with the company's OS4000 digital storage scope, acts as an interface between the scope and an output plotter. The 4002 is activated every time the scope stores a trace. It selects the printout condition and gives a single output trace at a speed pre-selected to suit the characteristics of the plotter. After completing a printout, the scope automatically resets to the "armed" condition and awaits a further input.

CIRCLE NO. 323



Unretouched photograph of screen.

# The Intecolor 8001 CRT. Buy One or Buy One Hundred. Just $1495.*

That's the price tag we'll put on the Intecolor 8001 if you place your order right now for 100 or more units. $1495. That's also the price we'll give you on a one-shot cash basis on an Intecolor 8001 CRT evaluation unit. Now, we'll never get rich with a price structure like that, but we look at it this way. That price is an investment in your future. We know that once you get your hands on the Intecolor 8001, once you see what it can do, you'll be back for more.

And it's because you'll be getting an Intelligent, 8-Color CRT that'll outperform any CRT on the market on a dollar for dollar and character for character basis. And it's complete. You won't have to lay out more cash for a keyboard, or 8080 CPU, or any of the standard features you'd expect to find on a good color CRT. It'll be ready to go. You can put it to work as a stand-alone CRT, incorporate it into your present system, or use it to upgrade the CRT's in the systems you're currently marketing. Whatever your application, it'll work for you.

But if your needs call for a more sophisticated CRT, a CRT that'll give you higher-level functions—no problem. We'll be glad to work with you to help you come up with an options package to fit your requirements. Like additional RAM to 32K, Roll, Background Color, Light pens, Graphics, 48 Line X 80 Characters/Line and up to 64 Special Graphics Characters. You define your needs, and we'll give you the capabilities to get the job done. It's that simple.

But if you'd like to see for yourself, look over our rep list on the adjacent page and ask the rep in your area for a demonstration. Whatever your application, he can show you the right Intecolor 8001 CRT at just the right price.

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Domestic U.S.A. prices

**CIRCLE NUMBER 57**

*INSTRUMENTATION*

## Smart analyzer computes power, gain, S/N

*Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, CA 94304. (415) 493-1501. $29,900; 120 days.*

Model 5420A "smart" digital signal analyzer operates over a 25-kHz bw, with a dynamic range of 75 dB. Resolution to at least 0.004 Hz can be achieved anywhere in the range. Significant features include absolute internal calibration in the user's choice of engineering units, digital band selectable or "zoom" analysis, fully annotated dual-trace CRT display with X and Y-axis cursors, digital storage of both data and measurement setups on a tape cartridge, and a random noise source to provide test stimulus.

**CIRCLE NO. 324**

## DMM operates 50 h on four 'C' cells

*Gould Advance, International Div., Raynham Rd., Bishops, Stortford, Hertfordshire, England. 027955155 Telex: 81510.*

Alpha III DMM has a full 1999 scale length. The 3½-digit display uses LEDs. Alpha III operates for more than 50 h from one set of four replaceable SP12 "C" cells. There are 25 ranges of ac and dc V, ac and dc current, and resistance. All resistive ranges are protected to 250 V rms. Typical accuracy is 1%.

**CIRCLE NO. 325**

## Tester checks out analog meters

*Jewell Electrical Instruments, Grenier Field, Manchester, NH 03108. (603) 669-6400. $700; 2-3 wks.*

Model 651A tests all important analog meter functions, including accuracy, tracking, linearity, sticks in travel, hysteresis and resistance. Standard features include automatic sweep for all meter ranges, four programmable test points, adjustable response time selector, and multiple test points for tracking and linearity. Full-scale accuracy is ±0.1%.

**CIRCLE NO. 326**

## Function generator works at 30 MHz

*Krohn-Hite, Avon Industrial Park, Bodwell St., Avon, MA 02322. (617) 580-1660. $895; 8 wks.*

Model 2000 30-MHz function generator provides sine, square, triangle, positive and negative pulses, positive and negative ramp waveforms, plus 100:1 symmetry control for pulse and sawtooth waveforms. Features include calibrated, pushbutton attenuator; 30-V pk-pk open-circuit output; 1000:1 external frequency control.

**CIRCLE NO. 327**

## Waveform recorder samples at 2 ns

*Biomation, 10411 Bubb Rd., Cupertino, CA 95014. (408) 255-9500. $12,500; 60 days.*

Model 6500 waveform recorder resolves input signal levels to 1 part in 64 (6-bit resolution) and stores signal samples at sample rates from dc to 500 MHz. The samples are digitized by an a/d converter and stored in a 1024-word, solid-state digital memory. Input amplifier bandwidth is dc to 100 MHz and input-voltage ranges are ±250 mV to ±5 V. Sampling rates run from 2 ns to 1 s per sample or an external time base can be used.

**CIRCLE NO. 328**

## Need more counts? Try a 4-digit DPM

*Fairchild Camera, 1725 Technology Dr., San Jose, CA 95110. (408) 998-0123. $121; stock.*

Model 40 10,000-count, 4-digit panel meter is designed for applications where resolution requirements are greater than those provided by a 2000-count, 3-1/2-digit DPM. The unit comes with either a 15-pin, dual-row connector or 8-pin terminal block. Features such as bit-serial, decimal-point selection and external hold are available from terminals provided at the connector.

**CIRCLE NO. 329**

## Word generator lets you pick your length

*Tau-Tron, 11 Esquire Rd., North Billerica, MA 01862. (617) 667-3874. $5500; 6-8 wks.*

Model MG-302 uhf serial data generator operates from 1 to 325 MHz and provides an RZ or NRZ serial data pattern in word lengths of 16, 32, 64, 128 or 256 bits. The unit features 600-ps rise/fall times, RZ/NRZ data selection, and baseline offset of 0.5 to −2 V. Programming is by front-panel data selection switches and address selectors.

**CIRCLE NO. 330**

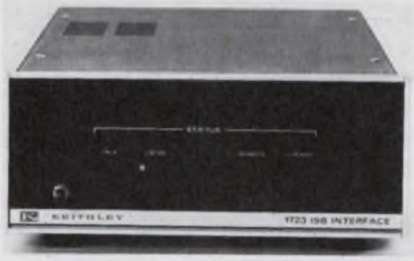
## Frequency counter sells for $150

*Simpson Electric, 853 Dundee Ave., Elgin, IL 60120. (312) 697-2260. $150; stock.*

Model 710 frequency counter covers 10 Hz to 60 MHz with 1-Hz resolution. Sampling is 5 times/s on the MHz range and 0.5 times/s on Hz. The display is a 6-digit, 0.35-in. LED readout with overrange indicator. Accuracy is ±1 count (±time base accuracy), with a 10-ppm time base. A switchable low-pass filter eliminates input noise. Size in only 2 × 5.6 × 4.6 in.

**CIRCLE NO. 331**

## Interface makes DMM IEEE-bus compatible

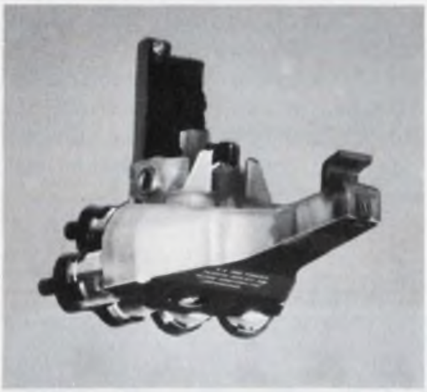


*Keithley, 28775 Aurora Rd., Cleveland, OH 44139. (216) 248-0400. $795.*

When combined with the company's Model 172 digital multimeter, the 1723 microprocessor-based interface provides a five-function, 30,000-count, 0.01% basic dc accuracy, IEEE Standard 488-1975 bus-compatible DMM. The 1723 provides the logic and control functions necessary to interface the Model 172 or 173 DMM. The unit provides $10^9$ Ω and 100-pF isolation from analog low to digital low.

**CIRCLE NO. 332**

## Seven dot print head does 110 characters/s



*Victor Comptometer, 3900 N. Rockwell St., Chicago, IL 60618. Nils Pederson (314) 539-8200. $59.50 (1000 qty.).*

Capable of printing at 110 characters per second, the 129-112 print-head mechanism uses a seven-dot format. Weighing only 9 oz, the print head is claimed to provide a 20% improvement in duty cycle over the company's standard model. The seven-dot print head produces any character and can even do graphics.

**CIRCLE NO. 333**

## Data recorder interface mates unit with 8080

*Tandberg Data, 4060 Morena Blvd., San Diego, CA 92117. Peter Gilbody (714) 270-3990. $800; stock.*

Although developed to interface an 8080 microprocessor to the company's TDC 3000 digital cartridge recorder, a special interface board is general enough to be compatible with other microprocessors. The recorder is bus structured and the interface can handle up to four drives in a daisy-chain. Contained in the 8080 interface are all the normal formatting functions plus the interface logic to the processor bus, eliminating the need for a separate formatter. Data transfer takes place with direct memory access. The controller/interface provides all necessary functions for address decoding, tape motion control, generation of proper block gaps, writing and reading of data, automatic generation of tape marks, high-speed search, etc. Communication with the external microprocessor is over an 8-bit bidirectional data bus, a 16-bit bidirectional address bus, and nine lines.

**CIRCLE NO. 334**

## Video RAM board mates digital bus to monitor

*Matrox Electronic Systems, P.O. Box 56, Ahuntsic Stn., Montreal, Quebec H3L 3N5. (514) 481-6838. $295; 2 to 4 wks.*

Compatible with Altair, Imsai and other similar bus organized microcomputers, the ALT-2480 interfaces the bus to a video monitor. On the input side the ALT-2480 looks like a 4 k × 8 static RAM with a 500-ns access time. The output is a video signal that provides 24 lines by 80 characters of upper and lower-case symbols. A jumper option permits operation at 40 characters per line and two pages. Any character may be displayed as normal, reverse video or blinking. Boards for 50 or 60-Hz systems are available.

**CIRCLE NO. 335**

## Video display controller mates with PDP-8 or 11

*Computer Technology, 6043 Lanton Ave., Oakland, CA 94618. Eric Wogsberg (415) 451-7145. From $765 (10 to 24 qty); 3 wks.*

Slipping into a PDP-8 or PDP-11 minicomputer card frame the Viuram-8 or L11 CRT interface shares memory with the mini. The interface boards provide a 12-line × 80-character display of the full upper and lower-case display. Five display modes are available—reverse video, half brightness, cursor, blink and blank. Refresh is done at 60 Hz and operation is either in the noninterlaced or interlaced modes. The monitor interface is an EIA RS170 composite-video signal for a 75-Ω line. Power requirements are 5 V at 2.2 A, 15 V at 20 mA and −15 V at 70 mA.

**CIRCLE NO. 336**

## Development system handles three μP families

*Intel, 3065 Bowers Ave., Santa Clara, CA 95051. Rob Walker (408) 246-7501. $13,390 (basic system), $300 (optional MCS-48 macro-assembler), $3350 (add on diskette drive); stock.*

The Intellec 888 System, an enhanced version of the Intellec MDS 800 System, has two to four times the on-line storage capacity of previous systems. It supports fully modular programming in both assembly language and PL/M, and covers the software development requirements of all three Intel-originated microcomputer families—the 8080, 8085 and 8048. The basic Intellec 888 package includes a million-byte diskette system expandable to 2 Mbytes; a complete Intellec MDS 800 system with full 64-k RAM; an interactive CRT display console; a resident PL/M compiler for the MCS-80 and MCS-85, and a diskette operating system that includes a macro-assembler and all other software development packages. Optionally available is a macro-assembler for the MCS-48 family.

**CIRCLE NO. 337**

## Speech processor does voice comparisons

*Heuristics, Inc., 900 N. San Antonio Rd., Los Altos, CA 94022. (415) 948-2542. $249 (kit); stock.*

Compatible with all S-100 bus computers, the SpeechLab processor board digitizes and extracts data from a speech waveform. It also applies pattern matching techniques to recognize the vocal input. In addition to bus compatibility with microcomputers such as Sol, Altair, and Imsai, SpeechLab can be used with any computer with the aid of a separate power supply and connector. The board comes with a 275-page laboratory manual, a 95-page hardware manual, a high-fidelity microphone, and three programs on paper tape.

**CIRCLE NO. 338**

## Complete programming system costs under $1000

*PROM Programmers, 601 Nandell Lane, Los Altos, CA 94022. Jerry Rampelberg (415) 948-0450. See text.*

Available for just $930, a complete PROM programming system for 2704/2708 UV EPROMs includes programmer, erase lamp and carrying case. A PROM can either be copied or data can be manually entered via several control switches and bit switches. Included in the programmer is a 1-k × 8 RAM that can simulate the PROM in the system and write directly to the microprocessor bus. Options include a hex keypad and display, RS-232 and TTY interfaces and a prober/handler interface for PROM manufacturers. The programmer measures 6 × 8 × 2.5 in. and weighs 5 lb. Programmers are also available for 1702A, 5203 and 5204 PROMs.

**CIRCLE NO. 339**

## 12 and 15-in. monitors handle 20-MHz inputs

*Ball Brothers Research, Electronic Display Div., P.O. Box 3376, St. Paul, MN 55165. George Wagner (612) 786-8900. From $150 to $250; stock.*

Available in 12 and 15-in. diagonal versions, the TTL-120 and 150 video monitors are designed for 7 × 9-dot matrix displays. The monitors have 20-MHz bandwidths and electronic horizontal video centering within the raster. Also included is an electronic vertical linearity control. Simple subassembly interconnects are designed so that an optional modular sync stripper board for EIA composite inputs can be added. Other options include high line rates, dynamic focusing and skip-scan capability.

**CIRCLE NO. 340**

## Bar code reader mates with RS-232 equipment

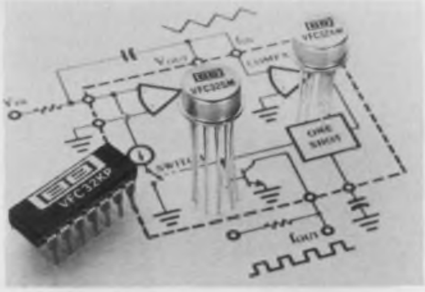
*Interface Mechanisms, 5503 232 St. S.W., Mountlake Terrace, WA 98043. Alison Grey (206) 774-3511. $1074; 30 to 60 days.*

Designed to scan universal product code symbols, the Model 9211 bar code reader handles UPC version A and E and EAN 13/EAN 8 symbols. All source printed colors that meet UPC symbol specifications can be read. The UPC reader includes the 1230R Ruby Wand, a visible (red) light pen for hand scanning. For remote applications, the Model 9211 is plug compatible with most CRTs and asynchronous communications terminals. The unit has dual connectors to allow tandem operation with any on-line RS-232C equipped terminal. External switches select baud rate, parity and half or full-duplex operation. The reader offers bit serial rates from 110 through 9600 baud.

**CIRCLE NO. 341**

## ICs & SEMICONDUCTORS

# V/f converter guarantees 12-bit linearity




*Burr-Brown, P.O. Box 11400, Tucson, AZ 85734. Joe Santen (602) 294-1431. See text.*

The VFC32 voltage-to-frequency converter guarantees ±0.01% (12-bit) linearity at 10 kHz and operation up to 0.5 MHz. The unit has a six decade range (0.5 Hz to 0.5 MHz) offering a top frequency linearity of ±0.2% (8-bit) and a 100-kHz linearity of ±0.05% (10 bits). An external RC network determines the full-scale frequency and an additional pull-up resistor and one-shot capacitor are also required for operation. An open-collector output makes this device DTL, TTL, and CMOS compatible. The unit is available in three models and two package configurations. Model VFC32KP is a 14-pin epoxy DIP specified from 0 to +70 C. The VFC32BM and VFC32SM versions come in a TO-100 package and are specified over the range of −25 to +85 C and −55 to +125 C, respectively. Prices (100 qty) are as follows: VFC32KP, $6.10; VFC32BM, $8.00; VFC32SM, $11.70.

**CIRCLE NO. 343**

# High speed transistors switch 1 A in 200 ns

*Kertron, 7516 Central Industrial Blvd., Riviera Beach, FL 33404. George Reiland (305) 848-9606. 100 qty. prices: $3.50 (6038); $3.10 (6039); stock.*

When used as a fast switch, the KS6038 and 6039 are capable of switching a collector current of 1 A on and off in a total switching time of 200 ns. To meet these conditions, the on time is 50 ns, storage time is 125 ns, and the fall time is less than 25 ns. When used as an amplifier the devices will have an $f_T$ of 300 or 200 MHz, when biased at a collector current of 500 mA and a collector voltage of 5 V, for the 6038 or 6039, respectively. Both transistors are housed in TO-60 isolated packages.

**CIRCLE NO. 344**

## Power Darlingtons switch in 400 ns

*TRW Power Semiconductors, 14520 Aviation Blvd., Lawndale, CA 90260. John Power (213) 679-4561. $6.45 (500 qty.); stock.*

The SVT6000 series of monolithic Darlington transistors can switch up to 500 V in 400 ns. They are npn devices, have a collector-emitter voltage range of 400 to 500 V and can withstand a continuous collector current of 15 A (peak currents of 20 A). Power dissipation for the devices is 96 W while the junction temperature range is −50 to +150 C. Sustaining voltage ratings for the SVT 6000, 6001 and 6002 are 300, 350 and 400 V, respectively. With a collector current of 15 A, the $V_{CE(sat)}$ for the three units is 2 V. Included in each device is a diode and resistor network to help speed the turn off. All units come in TO-3 cases.

**CIRCLE NO. 345**

## Video game circuits form programmable games

*Nortec, 3697 Tahoe Way, Santa Clara, CA 95051. Dick Kors (408) 732-2204. P&A: See text.*

A programmable video game chip set, called a video entertainment synthesizer (VES), can handle an unlimited variety of games. The basic game is designed for two players but expanded versions will allow up to four players to play either against each other or in competition with the VES "brain." In addition to an 8080 μP, two custom LSI circuits complete the system except for the program cartridges. All of the important variables of the VES output are under the control of the plug-in program. Seven color choices for the field, background and moving elements in the display as well as the audio output are all programmable. Both analog and digital inputs are accepted by the VES. Two, four-axis joy sticks provide the main analog inputs, and with the addition of another LSI circuit and controls, the number of primary inputs and players can be expanded to four. A light-pen input, usable with events occurring on the screen, can also be added. Three digital inputs, codable with eight discrete switches, permit program selection, handicapping, keyboards and other inputs.

**CIRCLE NO. 346**

## High current SCRs also operate at high temps

*Westinghouse Electric, Semiconductor Div., Youngwood, PA 15697. Woody Savage (412) 925-7272. $95.50 (10 to 99 qty); 6 to 8 wks.*

Able to operate at a 150-C junction temperature, the T625 series of high-temperature SCRs is designed to meet proposed NEMA motor overload standards. They have blocking voltage capability up to 1200 V and average current ratings of 250, 300 or 400 A.

**CIRCLE NO. 347**

## Two-chip set forms 4-1/2 digit a/d converter

*Siliconix, 2201 Laurelwood Rd., Santa Clara, CA 95054. Jim Graham (408) 246-8006. See text.*

Analog-to-digital conversion is stretched to 4-1/2 digits with the LD120 and LD121 IC chip set. The set offers high-impedence ($>10^9$ Ω) differential inputs and an accuracy specified to ±1/2 count of linearity. With the addition of a voltage reference, a one-transistor oscillator, some passive components and a display, the chip set makes a typical DPM system. Output levels are MOS and TTL compatible. The system employs quantized feedback. This produces a ratiometric response with respect to the reference voltage. The LD120 analog chip, a monolithic combination of PMOS and bipolar circuitry, comes in a 12-pin plastic DIP. The LD121 standard PMOS digital chip comes in an 18-pin plastic DIP. Prices (100 qty) are as follows: LD120, $6.43; LD121, $8.38; LD120/LD121 set, $14.81. Delivery is from stock.

**CIRCLE NO. 348**

## Switch 15 A at 400 V with these transistors

*RCA, Route 202, Somerville, NJ 08876. (201) 685-6423. From $3.96 (100 qty.); stock.*

The 9113 series of power transistors is designed for use in off-line power supplies. Included in the high-voltage, high-current series are the 9113, 9113A and 9113B. Top of the series is the 9113B, with a $V_{CEO}$ of 400 V, a collector current of up to 15 A, and a fast switching speed ($t_r$ = 1 μs and $t_f$ = 0.75 μs). Saturation voltages range from 1 V for the 9113 to 1.5 V for the 9113B. All three models come in TO-3 cases.

**CIRCLE NO. 349**

## Synthesizer provides 90 frequencies

*Hughes, 500 Superior Ave., Newport Beach, CA 92663. (714) 548-0671. $5.00 (1000 qty); stock.*

The HCTR0347 is a large-scale integrated CMOS digital frequency synthesizer aimed at CB applications. The unit provides receive and transmit frequencies for 45 channels using only one crystal for a reference frequency. Included are a programmable logic array that accepts binary, BCD, or 7-segment coded inputs, a programmable frequency divider, and a phase/frequency detector. The package is a 16-pin plastic DIP.

**CIRCLE NO. 356**

## 'Semicustom' circuits outpace other CMOS chips

*Master Logic Corp., 1623 Finch Way, Sunnyvale, CA 94087. Dr. Charlie Allen (408) 732-7777. See text.*

The Master Logic 200 family of logic arrays can be tailored by the manufacturer to custom configurations, though the basic chip is standardized. These "semicustom" CMOS chips offer twice the operating speed of competing CMOS circuits. Each chip has a maximum capacity of 200 gates of random logic or approximately 50 counter stages. Prototype development from customer logic drawings to working circuits takes 8 wks and costs $6600. Production prices range from $7 to $17, depending on quantity and package requirements.

**CIRCLE NO. 357**

## Monolithic d/a converter covers MIL temp range

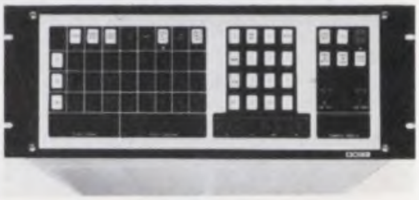
*Precision Monolithics, 1500 Space Park Dr., Santa Clara, CA 95050. Donn Soderquist (408) 246-9222. See text.*

The DAC-06 is a monolithic, two's-complement 10-bit d/a converter. It includes a precision voltage reference, R-2R resistor network, bipolar offset circuit, and a high speed (1.5-μs settling time) output op amp. Prices range from $15 for Model DAC-06GX (with a monotonicity and temperature range of 8 bits and 0 to 70 C, respectively) to $120 for the DAC06-883-AX (10 bits and −55 to +125 C). The latter version conforms to the MIL-STD-883A Class-B processing standard. The package is an 18-pin hermetic DIP. Delivery is from stock.

**CIRCLE NO. 358**

*DATA PROCESSING*

## μP-based system cues, syncs 3 tapes at once



*EECO, 1441 E. Chestnut Ave., Santa Ana, CA 92701. George R. Swetland (714) 835-6000.*

The μP-based series MQS-100 synchronizing system can cue and synchronize any three mag-tape transports (including video, audio and mag film) simultaneously. Tapes with drop-frame and nondrop-frame formats can be intermixed. Time-code readings for all tapes can be "captured on the fly," individually or simultaneously. The MQS fits standard 19-in. wide RETMA mountings with a height of 7 in.

**CIRCLE NO. 359**

## Computer accommodates 15 smart lab devices

*Digital Equipment, 146 Main St., Maynard, MA 01754. David Simler (617) 481-9511. From $14,000; August, 1977.*

A low-cost computer system, the DEClab-11/03 IB, supports up to 15 laboratory devices that use the IEEE Standard 488-1975. Fortran-4 programming is supplemented with a scientific subroutine package. Two versions are available, one employing an LA36 teleprinter as the terminal, the other using a VT55 video graphics terminal ($1000 extra). Both have floppy-disc storage, and a PDP-11/03 mounted in a small cabinet. Optional interfaces are available.

**CIRCLE NO. 360**

## Plug-compatible line printers save money

*Business Systems Technology, 3015 Daimler St., Irvine, CA 92714. Bill Wells (714) 549-9961. $15,000; 4 wks.*

Through a new controller, the entire family of BST chaintrain printers can interface directly to the Hewlett-Packard 3000 minicomputer, at speeds of 300, 425, 600 and 1000 lines/min. The 64-character set is standard, but sets of 96 characters are available. When purchased, the 600 line/min printer is said to save $2425. Or, the BST/600 can be leased for one year at $850 per month. The unit measures 42 × 36 × 26 in.

**CIRCLE NO. 361**

## Teleprinter uses μP for speed, versatility

*Tally Corp., 8301 S. 180th St., Kent, WA 98031. Horst Mader (206) 251-5552. From $3490; 16-20 wks.*

The Model T-1612, a low-cost 132-column teleprinter, is available in send/receive and receive-only versions. The bi-directional T-1612 uses an internal μP to print 160 char/s. Standard features include 300 to 9600 baud operation, parity checking, half or full duplex operation, data buffer (1-k characters), three serial interface configurations, bi-directional printing, 7 × 7 half-space matrix font, 96 printing characters (normal or double width), local or remote self-test, backspace, five-copy capacity and a slew rate of 8-1/2 in/s.

**CIRCLE NO. 362**

## Add-on memory includes protection and standby

*Electronic Memories & Magnetics, Computer Products Div., 3216 W. El Segundo Blvd., Hawthorne, CA 90250. (213) 675-9141.*

The 370/158 and 168 add-on memory systems include two unusual features, Standby Memory and deferred maintenance. Standby Memory includes 64 kbytes (in four 16-kbyte segments) of semiconductor memory and main-storage protection when double-bit errors occur. Deferred maintenance capability enables the operator to either automatically replace or reconfigure any failed segment of memory by using a single switch located on the front panel.

**CIRCLE NO. 363**

*PACKAGING & MATERIALS*

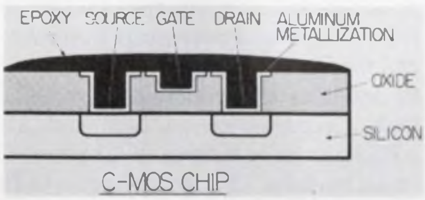
## Stock cases come in over 600 sizes

*W. A. Miller Co., Mingo Loop, Oquossoc, ME 04964. R. F. Hunger (207) 864-3344. $35 to $80 (unit qty); stock.*

Stock cases and enclosures, available off-the-shelf in a choice of over 600 sizes, range from 4 × 4 to 13 × 13 in. with depth variations up to 12 in. in increments of 1/8 in. Several styles of hardware are offered. Ruggedized construction features laminated wood with high-pressure decorative plastic laminate on exposed surfaces. All corners are internally reinforced with aluminum angle and bonded with epoxy adhesive.

**CIRCLE NO. 364**

## Opaque epoxy protects light-sensitive parts




*Epoxy Technology, Inc., 65 Grove St., Watertown, MA 02172. $15: 3-oz trial kit; stock.*

An opaque epoxy for coating light-sensitive components, Epo-Tek H62, is a thermally conductive, electrically insulating epoxy. A one-component system, the epoxy adheres well to ferrous, glass, ceramic and semiconductor materials. It comes as a thixotropic paste, easy to handle. A mechanical dispenser or simple syringe can dispense the material. The formulation requires no refrigeration in shipping or storage. Shelf life at room temperatures is up to six months and it cures rapidly at relatively low temperatures—30 min at 150 C, 60 min at 120 C. Volume resistivity is 1 × $10^{14}$ Ω-cm; lap shear strength is 1000 psi; operating temperature range is −67 to 300 F.

**CIRCLE NO. 365**

## Spray produces no-metal conductive coating

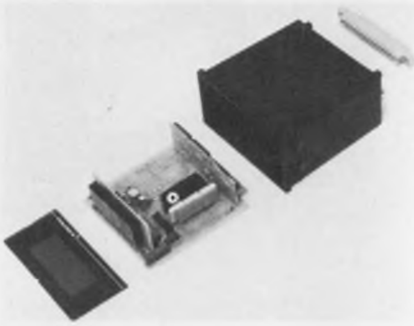
*Merix Chemical, 2234 E. 75th St., Chicago, IL 60649. (312) 221-8242. $21.60 gal. (60-gal.qty).*

Semiconductors requiring conductivity and ICs in need of zero-voltage readings can now have these characteristics with a conductive coating, antistatic No. 79. Free of metals, No. 79 achieves its conductivity chemically after it is diluted with de-ionized water 1:1. Wiped on, drying is instant, each gallon destaticizing and giving conductivity to an average 8000 to 10,000 ft².

**CIRCLE NO. 366**

*MODULES & SUBASSEMBLIES*

## DPM carries $39 price tag



*Analogic, Audubon Rd., Wakefield, MA 01880. (617) 246-0300. $39 (100s); stock.*

This 3-1/2-digit (±1999 count) DPI, the AN2570, offers accuracy of ±0.05% of reading ±1 count, bipolar differential input, a built-in, input-signal enhancement filter, and input protection of ±300 V dc or ac rms. All for just $39 in 100s. Bias current is 50 pA, input resistance is > 1000 MΩ, range tempco is ±35 ppm of reading/°C, and auto zero holds maximum zero drift to just ±1 μV/°C. Operating temperature is −10 to +65 C.

**CIRCLE NO. 367**

## Analog data modules mate with Exorciser

*Motorola Microsystems, P.O. Box 20294, Phoenix, AZ 85036. (602) 244-6815. $725/module; stock.*

Three Micromodule units give you Exorciser-bus-compatible a/d and d/a conversion. The MM5A and B are eight differential and 16 single-ended-input channel a/d converters, respectively. The MM5C is a 4-output-channel d/a. Input range of both the MM5A&B is ±10 mV to ±10 V and the amplifier gain range is resistor programmable from 1 to 1000. Both a/d's contain: an input multiplexer; a high-gain instrumentation amplifier; a sample/hold circuit; a 12-bit a/d converter; timing, control and address decode logic; and a +5 to ±15-V dc-dc converter. Throughput accuracy is ±0.025% of full-scale and conversion time is 33 μs. Analog output range of the MM5C is strap selectable. The d/a features output settling time of less than 10 μs and throughput accuracy of ±0.0125% of full scale.

**CIRCLE NO. 368**

## Rf amps star for range, noise and power

*Watkins-Johnson, 3333 Hillview Ave., Palo Alto, CA 94304. (415) 493-4141. $85 (1-9 qty); stock to 6 wks.*

TO-8 amplifiers—the WJ-A58 and the WJ-A59—provide max noise figures of 6.0 dB and 6.5 dB, and min output power of +18 dBm and +20 dBm, respectively. Both units feature a typical gain of 11 dB across the 5 to 500-MHz band. For the -A59, this yields a +117-dBm dynamic range in a 1-MHz bandwidth. The -A58 provides a typical third-order intercept point of +35 dBm while the -A59 has a typical intercept point of +38 dBm. These amplifiers operate from a 15-V-dc source.

**CIRCLE NO. 369**

## 14-bit a/d offers speed at low cost

*Analog Devices, P.O. Box 280, Route 1 Industrial Park, Norwood, MA 02062. W. Davis (617) 329-4700. See text; stock.*

Complete 14-bit a/d conversions are performed in 12 μs max by the ADC1131 (from $375, 1-9 qty) and in 25 μs max by the ADC1130 (from $275, 1-9 qty). Both successive-approximation devices convert analog input voltages into natural-binary, offset-binary, and two's-complement-coded outputs. Data outputs are provided in both parallel and nonreturn-to-zero serial formats. Although the 2 × 4 × 0.4-in. modules are available in versions with accuracies of ±1 LSB and ±½ LSB, max gain tempco is 10 ppm/°C on all modules. Operating from 0 to 70 C, the units miss no codes. Four input ranges can be programmed. The converters can be short cycled to perform conversions of less than 14 bits, with increased speed.

**CIRCLE NO. 370**

## 400-Hz Scott-T offers low profile

*Magnetico, 182 Morris Ave., Holtsville, NY 11742. H. Eicher (516) 654-1166. $22 (500 qty); stock to 8 wks.*

Line-to-line synchro voltages of 11.8 V rms, 400 Hz are converted to 2-V rms sine and cosine resolver voltages in the Model 13051, a Scott-T transformer. The printed-circuit-board mountable unit features a height of 0.25 in. Its other dimensions are 1.12 × 2 in. Conversion accuracy is 3 arc minutes.

**CIRCLE NO. 371**

## Regulated switchers deliver high current

*Power/Mate, 514 S. River St., Hackensack, NJ 07601. J. Geronimo (201) 343-6294. From $265; stock.*

The SW-G series of switchers offers six models with outputs from 2 to 28 V dc with ratings up to 40 A. Operating at efficiencies up to 84%, these 5-lb, 4.8 × 7.7 × 5.3-in. units deliver up to 200 W. The supplies operate from 85 to 132-V-ac and 170 to 264-V-ac inputs at 47 to 63 Hz, selectable from the front panel. Output regulation is maintained for 30 ms after loss of input power. All units are fully rated up to 50 C and regulation for both line and load is 0.1% with 25-mV pk-pk ripple.

CIRCLE NO. 372

## Tiny dc/dc converters hold tight regulation


*Integrated Circuits Inc., 16256 Northrup Way, Bellevue, WA 98005. (206) 747-8556. $61.50 (100-249 qty); stock to 4 wks.*

The series DCR-500 and DCR-1200 provide fully isolated (100-MΩ) ±12 or ±15-V-dc outputs from a 5 or 12-V input. The devices feature: load and line regulation of 0.03% and 0.05%, respectively; input-line ripple current of 4 mA rms; output noise of 2 mV rms; and output-voltage tempco of 0.01%/°C. Operating range is −20 to +71 C for the 0.75-oz units, which occupy 0.6 in³.

CIRCLE NO. 373

# Design aids

## Programmable memories

"Programming Handbook and Comparison Chart of Programmable Memory," a 32-pager, is a concise guide to all types of programmable memory. Data I/O. **CIRCLE NO. 374**

## TV camera tubes

Television camera tube sensitivities are compared graphically on a chart. Cohu, Electronics Div. **CIRCLE NO. 375**

## Linear circuits guide

TI's direct-replacement ICs for linear circuits produced by five other manufacturers are shown on a cross-reference chart. Texas Instruments. **CIRCLE NO. 376**

## Epoxy compounds

To find the epoxy compound with the properties you need, check a 16 × 10-in. selector guide. The guide lists electrical and physical properties at 25 C as well as handling and thermal properties for 22 epoxy compounds. Hardman. **CIRCLE NO. 377**

## Automatic screwdrivers

An automatic screwdriver reference chart offers a quick choice of screwdriving machines that automatically feed and drive any type standard screw. Weber Automatic Screwdriver. **CIRCLE NO. 378**

## Soldering materials

A short-form quick-reference selector guide describes solders, fluxes and chemicals. Multicore Solders. **CIRCLE NO. 379**

## Hexadecimal calculator

A hexadecimal calculator computes the offset for relative addressing as used by the 6800, Z80, 6502, SC/MP and F8 μPs; adds and subtracts hexadecimal numbers; calculates 2's-complements; and converts decimal to hexadecimal numbers and back. It is available for $3.95 (ppd) from E. & L. Pfeiffer, Computer Products, Box 2624, Sepulveda, CA 91343. **INQUIRE DIRECT**

# Vendors report

Annual and interim reports can provide much more than financial position information. They often include the first public disclosure of new products, new techniques and new directions of our vendors and customers. Further, they often contain superb analyses of segments of industry that a company serves.

Selected companies with recent reports are listed here with their main electronic products or services. For a copy, circle the indicated number.

**Sanders Associates.** Computer display terminal systems and related peripheral equipment; electronic and electromechanical products. **CIRCLE NO. 380**

**Beckman.** Analytical instruments, consumable chemical products and supplies and precision electronic components. **CIRCLE NO. 381**

**Amdahl.** Large-scale computers. **CIRCLE NO. 382**

**National Semiconductor.** Memory components and systems; μPs; MOS/LSI circuits; modules; linear and digital ICs; interface products, hybrids; optoelectronic products; discrete semiconductors; transducers, consumer products and point-of-sale systems. **CIRCLE NO. 383**

**Electronic Arrays.** Memory products, μPs and MOS/LSI circuitry. **CIRCLE NO. 384**

**Microdata.** Minicomputer products and systems. **CIRCLE NO. 385**

**Tektronix.** Information display products; oscilloscopes; modular instruments; spectrum analyzers; cable testers; medical electronics; TV products and logic analyzers. **CIRCLE NO. 386**

**Methode Electronics.** Electronic and automotive interconnection products. **CIRCLE NO. 387**

# New literature


### Microprocessors

A 40-page product guide covers ICs, support systems, and accessories that make up the CDP1800 COSMAC microprocessor family. RCA/Solid State Div., Somerville, NJ

CIRCLE NO. 388

### Motors and fans

Dc and ac miniature motors, fans, and blowers are featured in a 20-page catalog. TRW Globe Motors, Dayton, OH

CIRCLE NO. 389

### Data-conversion systems

A 180-page handbook, "The Analogic Data Conversion Systems Digest," Edition 1, is a no-nonsense collection of tutorial and reference material. Topics covered include parameter definitions and design considerations, effects of noise on a/d conversion, and reliability and testing of converters. The book costs $10.50. For further information, circle the reader service number. Analogic, Wakefield, MA

CIRCLE NO. 390

### Breadboard, test equipment

Breadboarding and test equipment is highlighted in a 16-page catalog. Continental Specialities, New Haven, CT

CIRCLE NO. 391

### LSI

All product and applications literature on LSI and micropower linear lines are contained in a catalog. Siliconix, Santa Clara, CA

CIRCLE NO. 392

*NEW LITERATURE*

## Sockets

High-reliability IC sockets, socketboard systems and IC-interconnect accessories are covered in a 72-page catalog. Robinson-Nugent, New Albany, IN

**CIRCLE NO. 393**

## A/d converters

A "minibrochure" describes the 6100 series of $\mu$P-compatible, multislope, integrating a/d converters. Specifications, prices, outline dimensions and pin connections are included. SGR Corp. Canton, MA

**CIRCLE NO. 394**

## PROMs

"PROM User's Guide," a 46-page book, covers tips on using bipolar, MOS, and TTL bipolar PROMs, with detailed programming articles on the 1702A and 2708 MOS PROMs. Pro-Log, Monterey, CA

**CIRCLE NO. 395**

## Desktop computer

The Hewlett-Packard 9825 desktop computer, designed for stand-alone computing or industrial and scientific system control applications, is featured in a 12-page data sheet. Hewlett-Packard, Palo Alto, CA

**CIRCLE NO. 396**

## Data-processing equipment

A 70-page catalog is divided into several sections which describe the functions, specifications, and appearances of dispersed-data-processing and business computing hardware. A companion software catalog is also available. Datapoint Corp., San Antonio, TX

**CIRCLE NO. 397**

## Minicomputer accessories

A 40-page catalog describes disc cartridges, magnetic tape, floppy discs, carrying cases, binders, connectors, cables, racks, and cabinets for all makes of minicomputers; plus unique and hard-to-find items for end users as well as OEMs. Minicomputer Accessories, Palo Alto, CA

**CIRCLE NO. 398**

## Fluorocarbon products

Illustrations, specifications, technical-property charts, and prices of plastics and fluorocarbon products are given in a 40-page catalog. Saunders Corp., Los Angeles, CA

**CIRCLE NO. 399**

## Electrolytic capacitors

Industrial-quality, miniature, aluminum electrolytic capacitors are described in an 8-page catalog. Murata, Marietta, GA

**CIRCLE NO. 403**

## Telecomm test equipment

The rental and lease of telecommunications and general-purpose test equipment is covered in an eight-page catalog. Leasametric, Metric Resources Corp., Burlingame, CA

**CIRCLE NO. 404**

## Data-comm products

Interfaces, cables, couplers and peripheral data-communication support products are shown in an 18-page catalog. Expandor, Monroeville, PA

**CIRCLE NO. 405**

## Electronic surplus

The "Clean-Sweep-Sale" catalog lists a vast assortment of electronics, optics and miscellaneous accessories. B&F Enterprises, Peabody, MA

**CIRCLE NO. 406**

## Microprocessors, ICs

Descriptions, application notes and diagrams of 12 microprocessors and ICs designed for telecommunication applications are given in a 12-page booklet. National Semiconductor, Santa Clara, CA

**CIRCLE NO. 407**

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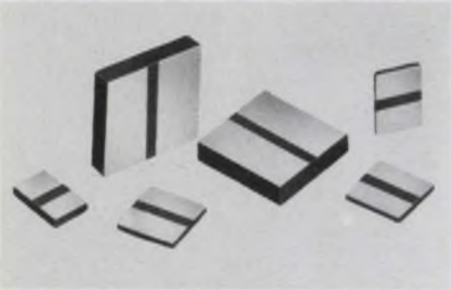
# quick ads

New and current products for the electronic designer presented by their manufacturers.



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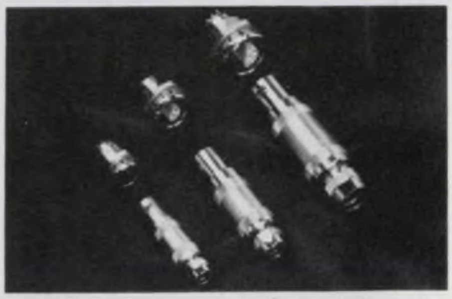
CERAMIC CHIP CAPACITORS 181



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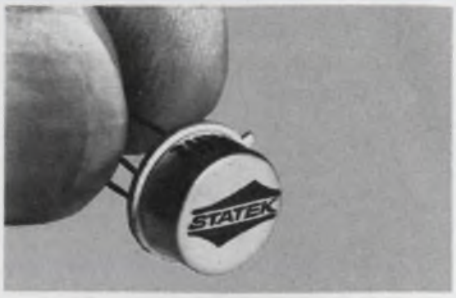
CONNECTORS 184

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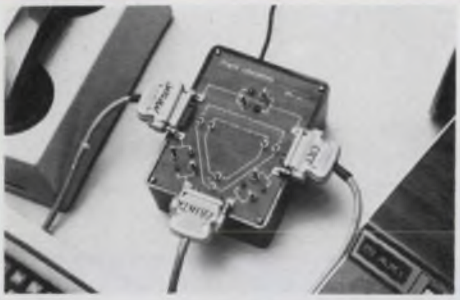

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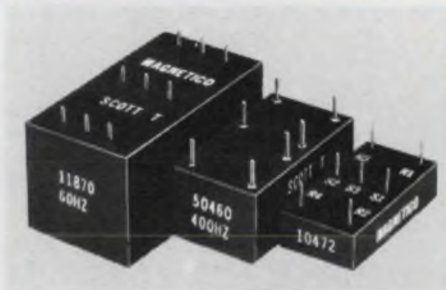
3 PORT RS232 & 20 MA LOOP 182

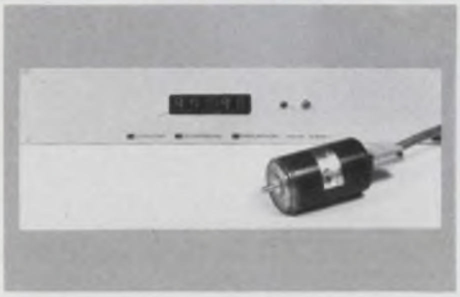

**INTEGRITY AND RECOVERY IN COMPUTER SYSTEMS,** by T. K. Gibbons. Here is a step-by-step guidebook that places at your fingertips all the techniques and strategies you need for locating and correcting errors and failures and for re-establishing complete system integrity and reliability as quickly as possible. #5454-8, 144 pp., $9.95. Circle the Info Retrieval Number to order your 15-day exam copy. When billed, remit or return book with no obligation. **Hayden Book Co., 50 Essex St., Rochelle Park, N.J. 07662.**

INTEGRITY & RECOVERY 185




Scott T Transformer. 11870: 60HZ, 90v, L-L in. 1.1x2.1x1.1. 50460: 400 HZ. 90v, L-L in. 7/8x1-5/8x11/16. 50642: 400HZ, 11.8v, L-L in. 7/8x5/8-11/16. 10472: 400-HZ, 11.8v, L-L in. 3/4x1-1/2x3/8. All with 6v RMS sine & cosine output. MAGNETICO, INC., 182 Morris Ave., Holtsville, N.Y. 11742 516-654-1166.

TRANSFORMER 188



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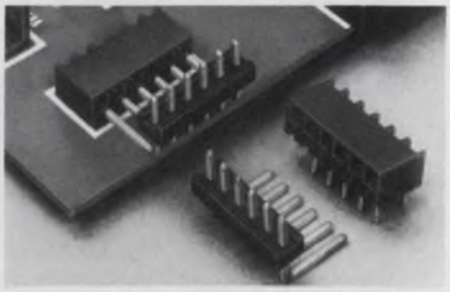

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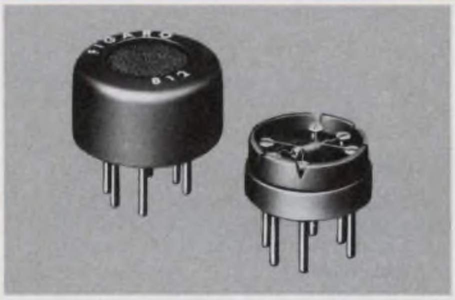

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GAS SENSOR 193


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IDEAS FOR DESIGN 191


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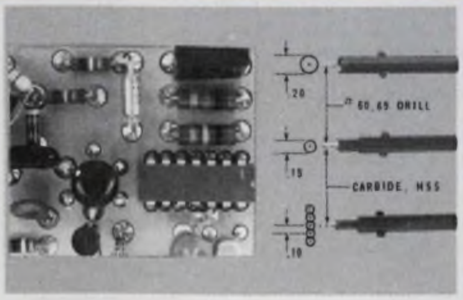


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**Advertisers in non-U.S. edition*

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# Product index

**Information Retrieval Service.** New Products, Evaluation Samples (ES), Design Aids (DA), Application Notes (AN), and New Literature (NL) in this issue are listed here with page and Reader Service numbers. Reader requests will be promptly processed by computer and mailed to the manufacturer within three days.



## design aids



## new literature

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# SuperTerm™

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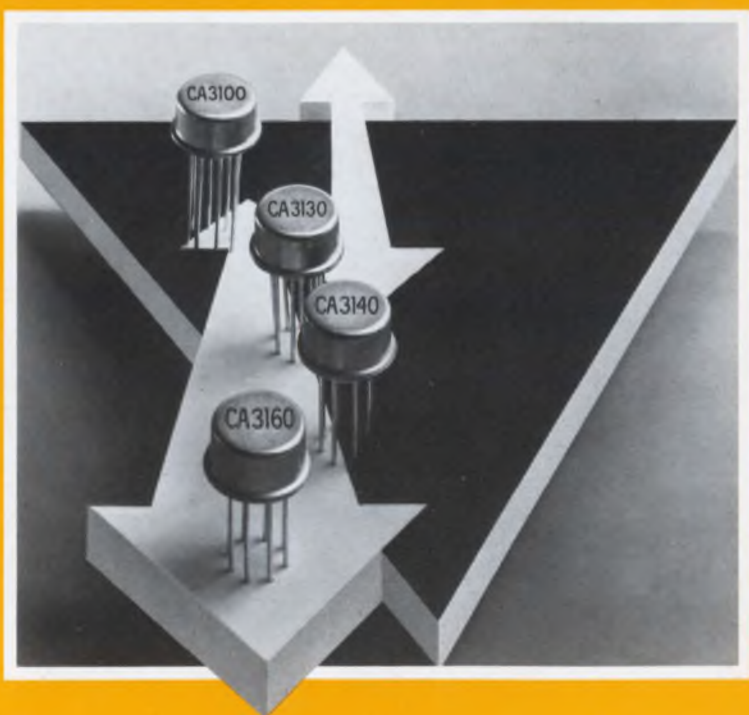


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